Day-1

15-Oct **AM** **Room AB (Century AB)**

Plenary Session					
Time	Paper #	Title	Speaker	Affiliation	Abstract
9:30	**Opening Remarks**		Shozo Saito	ISSM Organizing Committee Chair	
9:50	**Keynote Speech**		Shozo Saito	Toshiba	In the coming age of the Smart Community Society, we will have to make practical use of Big Data. Toshiba is the only company with capabilities in both semiconductors and storage products, a strong point that gives us advantages in developing and executing strategies for total innovation in storage. In recent years, Japanese companies have lost share in the world semiconductor market, as U.S. and Asian companies have increased theirs. We propose a business model of the sort required to revitalize Japan's semiconductor industry.
10:50	**Keynote Speech**	What did I explore in Half a Century of Research?	Dr. Leo Esaki	Nobel Prize Awardee / President, Yokohama College of Pharmacy/Chairman, The Science and Technology Promotion Foundation of Ibaraki	In 1947, after graduation in Physics, the University of Tokyo, I explored the possibility of putting quantum principles into practice in the electronics industry, which was a rather unique venture at that time. At Totsuko (presently SONY), Tokyo, in the course of tunneling study in narrowing the p-n junction width down to 10 nanometers, the Esaki tunnel diode - the very first quantum electron device - came as a total surprise in 1957. In recognition of this discovery the 1973 Nobel Prize in Physics was awarded. At IBM Watson Research Center, New York, we pioneered research on superlattices and quantum wells in the 1970s and the early 1980s, setting off a wide variety of experimental and theoretical investigations worldwide, resulted in not only the observation of a number of intriguing new phenomena such as Bloch oscillation due to electric quantization, but also the emergence of a new class of transport and optoelectronic devices such as high electron-mobility transistors (HEMT), high-speed resonant tunnel diodes, high-performance injection lasers with quantum wells, and quantum cascade lasers. In recognition of this invention, the APS 1985 Int. Prize for New Materials, the 1991 IEEE Medal of Honor and the 1998 Japan Prize were awarded. Since the superlattice periods or the quantum well-widths are on the nanometer scale, the studies have served as the precursor to a variety of nanostructures.
11:50	**Lunch**				
13:00	**The 20th Anniversary Speech**	- ISSM - Accelerator from "Know-how" to "Science"	Yasuo Mizokami	Japan General Manager, Molecular Imprints, Inc.	
13:40	**Highlight Session** **Process Control Solution** **Invited Talk**	Realities of Virtual Metrology	Prof. Costas J. Spanos	Andrew S. Grove Distinguished Professor, Electrical Engineering and Computer Sciences, University of California, Berkeley	

Day-1

15-Oct **PM** **Room A (Century Room A)**

Highlight Session : Process Control Solution					
Time	Paper #	Title	Speaker	Affiliation	Abstract
14:40	**PC-O-18**	Local overlay measurement and characterization for pitch-split double patterning process using CD-SEM	Shoji Hotta	Hitachi	Local overlay metrology technique using CD-SEM is applied to in-die overlay monitoring for pitch-split double patterning process. Overlay between pitch-split layers is measured on 32-nm lines/spaces pitch-split features located in a 7 ~7-um in-die metrology structure. Precision of CD-SEM overlay metrology is assessed by comparing with optical metrology, and CD-SEM metrology shows better precision at a small target size, which is required for in-die metrology application. Correlation between measured overlay and electrically measured capacitance difference of the pitch-split features is modeled, and good correlation is confirmed when CD-SEM metrology is used. CD-SEM in-die metrology can monitor overlay on a device with a precision of <1 nm when a metrology target is placed within ~1 mm from the device.
15:00	**PC-O-41**	A dynamic overlay sampling scheme for APC in high-mix fab	Chen-Fu Chien	al Tsing Hua University	Focusing on the challenges of production environment with multiple tools and products (high-mix) in modern semiconductor fabrication facilities (fab), this study proposed a dynamic overlay sampling scheme with underlying advanced process control to reduce the metrology cost in lithography processes while ensuring the quality level. An empirical study was conducted in a leading semiconductor company in Taiwan to validate the effectiveness of proposed approach. The results indicated that the proposed approach gained more sampling rate reduction compared to the existing sampling scheme. It also demonstrated the practical viability of the proposed approach.
15:20	**PC-O-4**	Multi-parametric Virtual Metrology Model Building by Job-shop Data Fusion Using a Markov Chain Monte Carlo Method	Kenji Tamaki	Hitachi	This paper proposes a generic methodology for building a multi-parametric virtual metrology (VM) model that predicts the Cu-CMP polishing rate in mass production of many different products in small quantities using multiple tools in a job-shop. The VM model must handle inter-individual differences in both products and tools with multiple parameters. To identify the multi-parametric VM model from datasets on small samples collected from the tools in the early stages of mass production, all the datasets are fused together using a Markov chain Monte Carlo method for a hierarchical Bayesian model.
15:40	**Author's Interview & Break**				
16:00	**PC-O-31**	Copper CMP APC for 32nm & 22nm Nodes Using Integrated Metrology	Lin (Larry) Yang	IBM	
16:20	**PC-O-54**	Bayesian Networks for maintenance planning in ion implantation	Ulrich Schöpka	Fraunhofer IISB	In this paper, the utilization of Bayesian Networks modeling for Predictive Maintenance (PdM) is described, and a PdM model for prediction of the filament breakdown in an indirectly heated cathode (IHC) ion source of an Axcelis GSD High Current Implanter is proposed. For this equipment, the most frequent maintenance task is related to the periodic breakdown of the heater filament or the cathode cap covering the filament within the source. By using Bayesian Networks modeling utilizing Soft Discretization, prediction models for the filament breakdown have been successfully created.
16:40	**PC-O-21**	Prediction and Control of Transistor Threshold Voltage by Virtual Metrology (Virtual PCM) using Equipment data	Tomoya Tanaka	Panasonic	This paper is a description of how to predict and control the transistor threshold voltage (Vth) by virtual metrology (VM), which we call gVirtual PCM, h by using equipment data. Impact analysis for Vth variation by using a Virtual PCM model indicates that the impact of source and drain (S/D) resistance and extension resistance are comparable with that of the shape factor (gate length, sidewall length). Virtual metrology models for the resistance were developed to control and predict Vth. As a result of the VM control, Vth variation was reduced by 28%. Moreover, in-process prediction of Vth was put into practical use.
17:00	**Author's Interview & Break**				
17:20	**Networking Session**				
17:40	**Reception**				

Day-1

15-Oct **PM** **Room B (Century Room B)**

MS·ES Session					
Time	Paper #	Title	Speaker	Affiliation	Abstract
14:40	**MS-O-34**	Static Capacity Planning and Scheduling Considering Product-Mix and Complex Tool Requirements in 300mm Semiconductor FAB	Youngkook Kim	Samsung	
15:00	**MS-O-88**	Observations of the semiconductor market and technology in the last 20 years	Keiji Horioka	Applied Materials	Equipment suppliers are watching the semiconductor and electronics markets very carefully. Figure 1 shows revenues of Wafer Fab Equipment (WFE) (1) and total semiconductor devices(2) for the last 20 years. The scales are adjusted tenfold for comparison. The total semiconductor market has grown almost linearly from $50B in 1990 to $300B in 2011. The WFE market has also grown from $6B to $34B. These curves are roughly proportional to each other. But WFE curve is the more volatile of the two. There are sharp peaks at 2000 and 2006 and steep valleys follow them. The business window is narrow and the WFE supplier must timely develop the required technology tools by anticipating customer needs.
15:20	**MC-O-62**	Real-Time Transfer Control Method for Linear Tools	Teruo Nakata	Hitachi	This paper describes a real-time transfer control method to produce a high throughput for the linear tools of semiconductor manufacturing equipment. We developed a transfer control method for calculating a transfer sequence producing a high throughput in advance for various process times and switching the transfer sequence during operation of the equipment. The developed method improved the throughput of the linear tools in 70% of the tested process time combinations. In the most improved case, the throughput was improved by 33%.
15:40	**Author's Interview & Break**				
16:00	**MC-O-75**	Effective Bottleneck Centric Allocation and Sequencing of Wet-bench and Furnace Tool Groups	Yu-Ting Kao	National Taiwan University	Effective scheduling of wet bench and furnace tools is important to operation efficiency of semiconductor fabrication, where furnace tool group may usually be a bottleneck. The major challenges come from the batching requirements, internal tool sequence, and waiting time limitations,which constitute the problem complexity. This paper develops a novel two-phase solution scheme, a bottleneck centric integrated allocation and sequencing method (BCIASM), to effectively integrate the sequencing and allocation for wafers processing by wet bench and furnace tools. Phase I focuses on producing a sequencing integrated furnace schedule by assuming a fine furnace model with internal robot sequencing captured but a coarse wet-bench model. The schedule determines individual furnace tool allocations to products and steps satisfying major sequencing constraints. Furnace tool allocations are then viewed as demands for allocating and sequencing wet bench tools in Phase II. An existing optimization tool is skillfully applied in both phases. Test results over problem instances extracted from real fab data show superiority of the method. BCIASM leads to near-optimal schedules, 6.58% higher utilization than a hybrid allocation scheme of optimization and manual adjustment, and significant mean waiting time reductions. As BCIASM requires less than 30 seconds of computation time to obtain the results, it demonstrates a good potential for both large size problems and applications to dynamic allocations.
16:20	**ES-O-6**	Zero Manufacturing Wastewater in ATM	Chai, Cheap LIam	Intel	"It's no longer enough to just produce a profit. Instead, we need to continually improve our manufacturing process, thereby reducing our burden on the environment and becoming an asset to the communities in which we live and work" quoted by Gordon Moore, Intel Founder. Intel recognizes that water is a critical natural resource that is of strategic important to our business and the communities. This paper discussed how Assembly Test Manufacturing (ATM) factories marching toward achieving Corporate Environmental Goal of reducing water usage by 20% from 2010 to 2013.
16:40	**Author's Interview & Break**				
17:00	**Networking Session**				
17:40	**Reception**				

Day-2

16-Oct **Room AB** **(Century AB)**

Plenary Session					
Time	Paper #	Title	Speaker	Affiliation	Abstract
8:00	**Registration**				
9:00	**Keynote Speech**	Technologies and Business Strategies of IT Industry in the Future	Yoon Woo Lee	Executive Advisor, Samsung Electronics Co., Ltd.	
10:00	**Keynote Speech**	Leading through the present, anticipating the future	Shizuo Igarashi	General Manager, Manufacturing and Technology, Texas Instruments Japan	From the decision to extend its manufacturing footprint with strategic foundry relationships to opening the industry's first dedicated 300mm analog wafer fab, TI has managed to lead through the dynamic and ever-evolving semiconductor market. Even through times of great chaos and uncertainty, such as the financial uncertainty in 2008/2009 and the devastating 2011 earthquake and tsunami in Japan, TI's ability to anticipate change and lead through crisis gives customers the assurance that TI will support them today and well into the future. TI's leadership in embedded processing and analog semiconductors is the result of the company's clear strategy and focus on providing customers the broadest, deepest semiconductor portfolio of innovative products, strong customer support through a global sales force and a manufacturing model that ensures continuity of supply in any market environment. Today, TI is well positioned to help its 80,000 customers unlock the possibilities of the world as it could be - smarter, safer, greener, healthier and more fun.
11:00	**Break**				
11:10	**Invited Talk -- 3DIC**	3D-Integrated Circuits Technologies -The History and Future-	Morihiro Kada	Association of Super-Advanced Electronics Technologies (ASET)	
11:50	**Lunch**				
13:10	**Highlight Session** **Printed Electronics** **Invited Talk**	All-printed organic transistors for large-area, flexible electronics	Dr.Tsuyoshi Sekitani	Research Associate, Quantum Phase Electronics Center and Department of Applied Physics, School of Engineering, The University of Tokyo	Recent research progress and future prospects of printed, flexible electronics for next-generation’ambient human/machine interfaces, utilizing molecular electronic material-based thin-film transistors, is reviwed. Especialy, here we described the fabrication of large-area, flexible active matrix organic LED pixel circuit on 10-・m thin-film plastics. The circuit that applies printed floating-gate organic transistors can compensate LED brightness variations and degradation for more than 6 months. The 230×230 mm2 printed active matrix circuit comprises 64×64 screen-printed organic 2-transistor-1-capacitor cells.

Day-2

16-Oct **PM** **Room A (Century Room A)**

UC▪PO session					
Time	Paper #	Title	Speaker	Affiliation	Abstract
14:10	**UC-O-87**	Manufacturing challenges of GaN-on-Si HEMTs in a 200 mm CMOS fab	Denis Marcon	IMEC	In this work, we report on the challenges related to growth and processing of 200mm GaN-on-Si wafers in a CMOS fab. We describe the Au free process we developed as well as how we assure wafer quality prior processing. For the first time, we analyze possible Ga contamination issue related to the processing of GaN wafers and we present the cleaning procedures we developed to avoid it.
14:30	**UC-O-46**	Ultra-Fine Particle Removal using Gas Cluster Beam Technology	Kensuke Inai	Tokyo Electron	In this study, the ultra-fine particle removal using CO2 gas cluster ion beam (GCIB) technology is investigated. The GCIB is incident on the sample at an angle of 0 with respect to the surface normal. The higher PRE can be achieved at the higher kinetic energy of the gas cluster. It is possible to remove the ultra-fine particle as small as 12 nm in diameter (which is required for 2014 by ITRS 2011). The pattern damage is not observed for 45 nm poly-Si pattern. Moreover, The molecular dynamics (MD) simulation is performed to investigate the mechanisms of the particle removal by GCIB irradiation.
14:50	**UC-O-85**	Study of airborne nanoparticle in cleanroom	Eri Uemura	Toshiba	
15:10	**Author's Interview & Break**				
15:30	**PO-O-92**	Nitrogen Profile Engineering for Scaling SiON Gate Dielectrics with Improved Interface Quality, Gate Leakage and NBTI Performance	Shenglin Wang	GLOBALFOUNDRIES	
15:50	**PO-O-95**	Effect of Cu CMP Pad Clean on Defectivity and Reliability	Leong Lup San	GLOBALFOUNDRIES	Effect and Mechanim of a pad cleaning process in reducing polish scratches were discussed. An additional advantage of the process is improved TDDB and a probable explanation was proposed
16:10	**PO-O-12**	MEOL Process Optimization for Low Cost TSV Fabrication	Ryohei Kitao	Renesas Electronics	To realize low cost TSV MEOL process flow, we examine direct deposition of bump metal on TSV in via-middle fabrication method. After Si wafer thinning and via-reveal, thin SiN and SiO2 films were deposited on TSVs and Si. Cu-reveal CMP was performed successfully remaining sufficient TSV height, followed by the direct deposition of BM was implemented. This approach resulted in eliminating several MEOL processes.
16:30	**Author's Interview & Break**				
16:50	**3miniutes Summary presentation by Interactive Poster Speaker**				
17:40	**Break**				
17:50	**Poster Session**				

Day-2

16-Oct **PM** **Room B (Century Room B)**

DM▪PC▪PE Session					
Time	Paper #	Title	Speaker	Affiliation	Abstract
14:10	**Highlight Session** **Printed Electronics** **Invited Talk**	Conductive paste for Flexible electronic application	Takayuki Ogawa	Harima Chemicals	In recent years, touch screen panel market has been rapidly expanding as mobile devices become increasingly popular. Touch screen panel is mainly formed by transparent electrode which detects a signal from the external and metal wiring which drives the transparent electrode on the flexible circuit. The conductive pastes applied to the metal wiring were continuously developed by optimization of matrix polymer and conductive filler. The newly developed conductive paste enabled the formation of the fine pattern with 50μm width on PET film by screen printing. Moreover, in the case of gravure offset printing, we have succeeded to pattern the 40 μm line by controlling the affinity between the conductive paste and blanket roll.
14:30	**DM-O-90**	Designer-Friendly Half-Node Strategy of Logic Technology Based on Precise Yield-Aware Management of Lithography Misalignment	Satoshi Nakai	Fujitsu Semiconductor Ltd. (Fujitsu Microelectronics)	We demonstrate sophisticated methodology of optimizing an SRAM-cell shrinkage for a half-node logic technology based on contact-layer-misalignment-related SRAM yield as a function of lithography-cost increase. In addition, our half-node technology of 55nm features designer-friendly strategy of SPICE compatibility with the parent technology of 65nm.
14:50	**PC-O-5**	Advanced thermal budget monitoring technique for spike annealing.	Nao Higuchi	Renesas Electronics	With the scaling of devices, the thermal budget control of spike annealing has become more important to obtain high production yield. A novel thermal budget monitoring technique is proposed to assist the wafer temperature monitoring with pyrometers used in typical RTP tools. Time integration values of lamp power during spike RTA correlate with the measured sheet resistance of quality control (QC) wafers and predict a long term trend of thermal budget variation of product wafers. This technique can realize a robust spike RTP process for advanced LSIs.
15:10	**Author's Interview & Break**				
15:30	**PC-O-81**	Resist patterning error detection technology of macro inspection tool for periphery of NAND Flash	Makoto Oote	Toshiba	Major memory makers have already implemented macro inspection tool to detect resist patterning error for ADI (After Develop Inspection). However, periphery area, which has much of random pattern and is relatively smaller than memory cell area, is often excluded from macro inspection. Periphery pattern error is currently detected only after etch/CMP, therefore, how to reduce time to feedback to the litho tools is the challenge. In this study, we developed and evaluated a new algorithm to detect resist pattern error on periphery at ADI with high sensitivity. New algorithm automatically learns information of programmed resist pattern error on periphery and reference (normal shot) and uses image difference to detect pattern error.
15:50	**PE-O-68**	Wafer Edge Region Cleaning by Wet Blasting	Akira Shiraishi	Raytex	We have developed a new wafer edge region cleaning system due to the high demands for a non-selective treatment that removes all materials, such as meal High-k dielectrics stack films and reduce their total cost of ownership. The unique feature of our system development is the use of an abrasive wet blasting method. This study investigates an initial feasibility of wafer edge bevel treatments through the new technique. We concluded that the wet blasting approach could easily remove multiple film layers on a device wafer edge zone in a really short period of time. We already conducted demonstration experiments to verify the effectiveness of the wet blasting practice not only typical edge cleaning procedure but also edge trimming application for the TSV manufacturing process.
16:10	**PE-O-70**	Measurement of Leakage Current Conductivities in Ultra-Thin Gate Dielectric using Non-destructive and Contactless Technique	Justin NDAGIJIMANA	Kumamoto University	
16:30	**Author's Interview & Break**				
16:50	**3miniutes Summary presentation by Interactive Poster Speaker**				
17:40	**Break**				
17:50	**Poster Session**				

Day-3

17-Oct **AM** **(Century AB)**

Plenary Session					
Time	Paper #	Title	Speaker	Affiliation	Abstract
9:30	Keynote Speech	European Vision and Achievements Towards Larger Diameter Wafers	Prof. Dr.. Lothar Pfitzner	Fraunhofer Institute for Integrated Systems and Device Technology IISB	
10:30	Keynote Speech		TBA		
11:30	Lunch				
12:50	Invited Talk Power Device	Recent progress of SiC power device	TBA	Mitsubishi Electric	For the realization of the low-carbon society, development of energy-saving and new energy technology are demanded. A power electronics technology was a key technology for energy saving, and the continuous improvement in performance of the Si power device has been accomplished. The SiC power device surpasses a Si power device by its physical properties. Recent years, the development of the power device using SiC became popular, and part of product which applied SiC power device came up in the market. In this presentation, I will report the progress of SiC power device and power module which applied SiC power device.
13:30	Highlight Session BCP Invited Talk	On-site Earthquake Early Warning System for Semiconductor plant	Kenichi Takamatsu	Oki Engineering	On-site Earthquake Early Warning System (On-site EEW) has been developed to minimize the damage of semiconductor manufacturing plant. In addition, we created effective warning system against epicentral earthquake by improved the calculation methods. This system was able to minimize the damage at The 2008 Iwate Miyagi Nairiku Earthquake, further was functioned effectively in The 2011 off the Pacific coast of Tohoku Earthquake. Using this system is able to shut down special gases, chemicals and to stop production before S-wave arrival. In business continuation program, On-site EEW is effective to reduce the damage and protect the lives of employee.

Day-3

17-Oct **PM** **Oct 17 PM (Century A)**

Time	Paper #	Title	Speaker	Affiliation	Abstract
14:30	**MS-O-37**	Quake resistance improvement of wafer Fab learned from Great East Japan Earthquake	Hidehiko.Kawaguchi	Renesas Electronics	This paper reports on new Renesas quake resistance imprpvement from Great East Japan Earthquake experiences. Great East Japan Earthquake hit Naka factory on Mar.11th, 2011. The earthquake acceleration reached 922gal on the surface of Naka ground. No one was hurt and leakage of gases and chemicals and a fire did not occur in the clean rooms. However, a certain number of the production tools and facilities had damaged because our quake resistance specification was 400gal that established by past earthquake experiences. By strong support, we could resume production on June 1st. That was for 3 months earlier than originially estimated. However, we made delivery shortage to our customers. To settle this problem, we established quake-resistance reinforcement technology which assures the recovery of a wafer fab immediately after an earthquake. This technology becomes a foundation of the new BCP.
14:50	**FD-O-17**	Anti-seismic measures of polyvinyl chloride (PVC) duct and clean room system ceiling	Akinori Kawasaki	Renesas Electronics	By investigating actual damage of The Great East Japan earthquake on 3.11 and considering BCP, we reconsidered anti-seismic measures and standard of PVC duct and clean room system ceiling. Those are, for PVC duct, to strengthen rigid support and to insert flexible ducts newly, and for system ceiling, to add diagonal braces and to install vertical braces newly. And we carried out actually shaking experiment to verify these measures f effect. We could not experiment at KH=1.0 (expected seismic intensity) for the safety of experiment facilities, but we verified the effect of these measures and got prospect to withstand at KH=1.0.
15:10	**ES-O-58**	Seismic Anchorage for Wafer Process Tools Capable for Severe Earthquake	Shoji Ishida	Renesas Electronics	An anchorage method for wafer process equipment against strong seismic vibration is described in this paper. The basic concept was established by our experience of the Great Hanshin Earthquake in 1995 and was verified how it worked against the Great Eastern Japan Earthquake in 2011. After that it has been further improved to minimize process equipment damages. Three detail implemented measures are introduced in this paper.
15:30	**FD-O-33**	Wafer Carrier Fall-Off Protection Implementation for Automated Stokers	Michiyuki Shimizu	Renesas Electronics	
15:50	**Author's Interview & Break**				
16:10	**YE-O-55**	Yield Improvement by Identifying a Precursor NVD as the Root Cause of Electrochemical Induced Pitting Defects at Gate Oxide Patterning	Jungtae Park	Samsung	
16:30	**YE-O-79**	STI Crater Defect reduction for Semiconductor Device Yield Improvement	Liang Li	GLOBALFOUNDRIES	One type of yield killing defects called “STI Crater” were found on advanced CMOS devices during STI formation. Various cleaning and thermal treatment applications have been evaluated to eliminate the defects for yield enhancement.
16:50	**YE-O-014**	Modeling with FDC data for yield enhancement	Yi-chun Chen	TSMC	The concept of fault detection classification (FDC) is to detect changing conditions of the equipment properties and to improve process by using the information and knowledge, detected. FDC data herein are historical data of equipment and process parameters collected from FAB and transformed into new variables. This study presents a FDC-based model methodology to construct the relationship between FDC data and the response of interest by a two-stages analytical flow. Tthe rolling data in the second stage would be analyzed and tested against the model built in the first stage, off-line training process, in order to detect the timing that the model should be refreshed due to worse prediction quality of the model. This work improves (1) the efficiency of data collection, (2) accuracy, robustness, and fitting and prediction performance of model, (3) reduction of users' effort of monitoring and checking causes of alerting.
17:10	**Author's Interview & Break**				

Day-3

17-Oct **PM** **Oct 17 PM (Century B)**

PO Session					
Time	Paper #	Title	Speaker	Affiliation	Abstract
14:30	**PO-O-27**	Fluoride Contamination Induced NiSi2 Film Formation in a Gate NiSi Line	Takuya Futase, PhD	Renesas Electronics	Undulate, high-resistance nickel silicide film wasfound in a gate electrode of logic device. The undulate film was caused by fluoride contamination derived from a chemical dry-cleaning for silicon substrate prior to nickel sputtering. The nickel silicide film was composed of a thicker nickel monosilicide (NiSi) and a thinner nickel disilicide (NiSi2) film. We hypothesized that fluoride contamination retareded nickel diffusion during the initial silicidation; thus, the thin silicide film transformed into NiSi2 because of excess thermal budget during the second silicidation.
14:50	**PO-O-16**	Quantification and solution of wafer sticking in pattern plating	Shinsuke Kozumi	Renesas Electronics	In this paper, we report on quantification and solution of wafer sticking in pattern plating. We developed coupon test to quantify the adhesion strength of sticking, and evaluated lithography and electroplating process condition dependence. We found out that increasing photoresist bake temperature causes increase in the photoresist hardness, resulting in reduction of the adhesion strength. Considering our quantitative results, lithography and electroplating process performance, we optimized the photoresist bake condition, and eliminated wafer sticking successfully.
15:10	**PO-O-74**	Optimization of a 65nm Back Illuminated CMOS Image Sensor by Varying Implant Angle	YU WEI MING	TSMC	The device of interest in this study is a 65nm process technology fabricated back-illuminated CMOS image sensor (BI-CIS). In this study, we investigated the implants for the main photon capturing region of the pixel structures, and their effects on white pixel (WP), full-well capacity (FWC) and image lag. Trade-offs between the key device parameters are readily seen with different choices of implant conditions. A multi-wafer type of implanter was chosen for this study. At the implant angles of interest, where the device performance could be optimized, there appears differential channeling of the dopant across the wafer. The process optimization technique for the elimination of differential channeling effects on the multi-wafer high-energy implantation systems is presented.
15:30	**PO-O-59**	Control of Trench CD's Variations in a Deep Trench RIE	Takayuki Sakai	Toshiba	– In a Si trench RIE for super junction formation, optimization of the process parameters which control the variations of the trench CDs within the wafer and the etch rate were studied. Multivariate analysis was carried out for the result of the DOE and the model formulae were derived using hyper-regression optimization method. It was shown by using this model that a parameter design which controls the variations of the trench CDs within the wafer and the etching rate is possible.
15:50	**Author's Interview & Break**				
16:10	**PO-O-40**	A Method of Clarification for Process Window of Cu Barrier/Seed for Void-Free Cu-Lines	Kazuyuki Omori	Renesas Electronics	To achieve void-free Cu filling, an optimization method to clalify the process window of Cu barrier/seed process is proposed. Using top-view SEM images after Cu seed deposition, a threshold value of opening width for void formation is determined. By using the threshold value, we can easily clarify the process window of Cu barrier / seed whose parameters increase in advanced Cu-lines.
16:30	**PO-O-9**	New Approach for Contact Dry Etch Process Optimization	Hiroyuki Yazawa	Renesas Electronics	We evaluated a new approach to quantify an incident rate of smaller critical dimension (CD) by CDSEM for optimizing etch process and yield improvement in this paper. Through the evaluation, we revealed that the approach was effective for contact etch process optimization to improve contact hole CD variation and yield.
16:50	**PO-O-8**	Optimization of groove structure for Cu-CMP pad	Shinichiro Kakita	Renesas Electronics	In a Cu-CMP process, there is an issue that by-products of slurry and Cu are accumulated in grooves of a Cu-CMP pad. It causes low removal rate and Cu residue. Thus a CMP pad has to be changed in shorter period than we expected. In order to prevent accumulation of the by-products and to extend pad lifetime, we tried to widen and deepen pad grooves. In that process, it was found that removal rate has a strong correlation with groove volume and surface area of a CMP pad.
17:10	**Author's Interview & Break**				

Day-2

16-Oct **3mins Summary Presentation** **(Century A)**

3 minutes summary presentation by interactive poster speakers				
Paper #	Title	Speaker	Affiliation	Abstract
FD-P-47	Facility Design through the Virtual Fab Simulation	Toshikatsu Masuda	Toshiba	The virtual fab simulation was developed to design the utility facility accurately. The accuracy of the simulation method was evaluated in the case of de-ionized water (DIW) consumed in the existing fab, and showed good accuracy. The method enabled to calculate the appropriate amount of utility in the case that the tool utility changes significantly. The collected data enabled to analyze the DIW usage, revealing that not a little amount of DIW was consumed in other than wafer processing.
MC-P-57	The Principle of Cycle Time Worsening in Semiconductor Logistics	WATANABE Hiroe	Panasonic	We have found the principle of Cycle Time worsening in such a complicated semiconductor logistics. In this paper it is explained by simple simulator based on cellular automata theory in the case of existing bottleneck equipment and re-entrant flow shop. As a result, cycle time can be considered algebraically as if it is electric circuit and it is easy to find the countermeasures to improve cycle time.
MC-P-60	Novel dispatching rule for re-entrant flow control in Q-time constraints processes	Akihiro KOBAYASHI	University of Tsukuba	This paper presents a new method (Synchronized-CKB with REFS) to manage Q-time constraints processes of an actual plant [2], while observing multiple Q-time constraints that interfere with each other, for the purpose of maximizing throughput, reducing the cycle time while sustaining maximum throughput. This method, achieves satisfaction of all Q-time constraints, increased throughput of quality products, shortening the cycle time, and reducing WIP. In addition, we have obtained results compared to [2], under the same conditions, the average waiting time can be reduced about 60-80%. In dynamic condition, this method achieves keeping Q-time constraints of all lots.
MC-P-61	Optimal Control of Engineering Operations on Production Tools in Semiconductor Manufacturing	Naoto TOYOSHIMA	University of Tsukuba	This paper presents a new method combined maintenance scheduling and lot scheduling to achieve high OEE and a short cycle time. New method named JAMP-wS can simultaneously schedule setup operation, maintenance opereations, and lot loading. Averaged and longest waiting times of lots were much shortened with JAMP-wS because of low WIPs and zero lots exceeded Q-time constraints. As the result the high OEE is achieved.
UC-P-24	Reduction of Bevel Particle Induced by Wafer Backside Chemical Cleaning	Pierre Loisel	TSMC	
YE-P-29	Applications of Electron Tomography for Semiconductor Failure Analysis and Reference Metrology	Hugh L. Porter	SEMATECH	In this paper, we report an electron tomographic reconstruction showing interfacial roughness between a titanium nitride and hafnium oxide film and an electron tomographic reconstruction of a backend metallization defect in a plan-view transmission electron microscopy (TEM) sample. The first example illustrates a low throughput reference metrology application, whereas the second illustrates a typical higher throughput yield enhancement application. Throughput in semiconductor applications, as it relates to ideal tomography applications, is discussed, contrasting the two examples.
YE-P-45	Intelligent Classification of Complicated Water Bin Map Patterns	Chia-Yu Hsu	National Tsing Hua University	This study proposes an intelligent approach to classify the complicated wafer bin map (WBM) with various pattern size, density, noise degree, and wafer rotation. First, spatial randomness test is used for each WBM to classify into random, repeat and cluster. Then, signal enhancement and noise reduction is applied for cluster WBM. Next, wave features from a spatial correlogram is extracted to build a classification tree for WBM classification. Based on the real setting, a simulated data sets were conducted to validate proposed approach. The results show that the proposed method is better than dynamic time warping classification approach.
YE-P-63	Knowledge searching system for particle cause	Hidefumi Matsui	Tokyo Electron	
PE-P-23	A novel method of PECVD film uniformity improvement by nitrogen carrier gas implement	Chung-Min Lin	TSMC	Oxy-nitride film SiON has the specific optical constant RI (refraction index= n+ik) to enhance lithography window to improve critical dimension control. At the offline monitor of PECVD chamber, SiON (ARC) film often suffers relative high out-of-control limit rate due to its rapid thickness uniformity trend-up phenomena with chamber PM wafer counts to cause poor thickness uniformity performance. To improve SiON film thickness uniformity, implement nitrogen gas as partial carrier gas into PECVD SiON process to achieve more well-mixed utility then further improve PECVD film with better thickness uniformity is the effective uniformity improved method.
PE-P-44	Plasma chamber corrosions by earthquake	Tsuyoshi Moriya	Tokyo Electron	After the Japan fs big earthquake in 2011, the plasma etching tools received the big influence of the quake. Most of the etching equipment was not able to be used normally. Many particles were produced and contaminated the silicon wafers during etching process because the chambers were corroded by the outgassed acids during shutdown for several days.

Day-2 **16-Oct** **3mins Summary Presentation** **(Century B)**

3 minutes summary presentation by interactive poster speakers				
Paper #	Title	Speaker	Affiliation	Abstract
PO-P-15	Particle reduction in etching tool re-startup from earthquake	Toshikazu hanawa	Renesas Semiconductor Engineering Corp.	In re-start up of etching equipment from the Great East Japan Earthquake, recovery efforts were jammed by particle generation. Shut down of clean air circulation affected environmental particles and other problems occurred in process chamber. It was important to confirm particle behavior and prepare procedure for scouting particle source on a normal basis. NPPC and temperature acceleration are effective and useful tools to accelerate recovery works.
PE-P-7	Quick Recovery of damaged clean room from quake hits	Fumihiko Matsuoka	Renesas Electronics	Quick recovery of Renesas Naka factory attacked by great earthquake hits is described in this paper. Facility system and production Equipment in clean rooms had damaged. We started restoration works with hundreds of hardware specialist. After 30 days from the disaster, all facility system recovered. Production machines were ready for test run after two weeks from facility system recovery. In order to remove defects, we cleaned up production equipment repeatedly and calibrated wafer transfer system. We believe that the cleaning and calibration procedures contributed to the quick recovery.
DM-P-49	Pattern variation analysis using vision system based on higher-order local auto-correlation	Tetsuaki Matsunawa	Toshiba	Although lithography conditions have been determined to obtain hotspot-free wafer image, those are still often found on a wafer. This is because the lithography conditions are optimized with limited variety of patterns. One of the ways to avoid hotspots is to verify enormous variety of patterns before mask making. This, however, is quite time consuming and cost inefficient. This paper proposes a new method to analyze and create a group of patterns to cover pattern variations in a chip layout based on Higher-Order Local Auto-Correlation. By verifying the proposed generated patterns, the lithography conditions can be optimized efficiently and dramatically reduce the number of hotspots.
PO-P-38	Study on characteristics of ALD oxide of new Si precursor for DPT application	Jun-Hyun Cho	Samsung	
PO-P-76	EUV Resist Material and Process Development at EIDEC	Eishi Shiobara	EIDEC	
PO-P-77	EUVL resist pattern formation: an in situ analysis using HS-AFM	Julius Joseph Santillan	EIDEC	
PO-P-80	New SiC Power Device and Module Developments	Tristan Evans	ROHM Co.,LTD	In this paper, two new Silicon Carbide (SiC) device structures and a new, full SiC module are presented. The MOSFET and diode developed for this work both utilize state-of-the-art trench structures resulting in increased efficiencies. The double-trench MOSFET developed by this group has achieved a class-leading low on-resistance while eliminating problems associated with gate oxide destruction at the trench bottoms. Likewise, the trench structure of the Schottky Barrier Diode (SBD) allows for reduced electric field at the Schottky interface and a reduced forward voltage drop without significantly altering the drift layer. Additionally, a transfer-molded power module utilizing a new high temperature encapsulation resin and incorporating the double-trench MOSFET has been developed. When compared to traditional, case type modules, this module represents a volume reduction of 13:1 as well as improved overall efficiency.
PC-P-19	Detection of Micro Arc Discharge Using ESC Wafer Stage with Built-in AE Sensor	Yuji Kasashima	National Institute of Advanced Industrial Science and Technology (AIST)	In order to detect micro arc discharge occurring around a wafer, we have developed the ESC wafer stage with a built-in AE sensor. The built-in AE sensor can detect the acoustic waves due to the micro arc discharge with high sensitivity. The results demonstrate that the novel ESC wafer stage with a built-in AE sensor is very effective to detect micro arc discharge occurring around a wafer and will extraordinarily contribute to upcoming manufacturing technology and improvement of current productivity in semiconductors.
PC-P-36	Excursion Reduction and Prevention Methodology	Charles chen , Cougar C	Xilinx	In current advanced 12 inch semiconductor foundry fab, an excursion can cause serious crisis to yield and product delivery besides consuming significant engineering resources to assess impact and contain the excursion. With complicated process steps and over hundred types of equipments used in today advanced process manufacturing, stable equipment performance is very critical for defect detection & yield stability. Fundamental tool management at foundry fab is essential for excursion prevention. A major part of Fundamental tool management methodology need timely feedback from product yield and diagnostic data to accurately identify highly problematic tools. Close partnership between design house and foundry fab can accelerate this learning and lead to more timely and more effective excursion prevention program.
PC-P-48	Development and Evaluation of Engineering Information System for Semiconductor Wafer Manufacturing	Naoki Kawamura	Renesas Electronics	
PC-P-104	Integrated Metrology for Advanced Lithography Process Control	Paul Luehrmann	ASML	