ISSM 2024

International Symposium on Semiconductor Manufacturing

December 9 - 10, KFC Hall, Ryogoku, Tokyo

Co-Sponsored by
IEEE Electron Devices Society, Minimal Fab, Semiconductor Equipment Association of Japan (SEAJ), Semiconductor Equipment and Materials International (SEMI) and Taiwan Semiconductor Industry Association (TSIA)
Endorsement by The Japan Society of Applied Physics (JSAP)

December 9 (Day-1)

JST(UTC+9)	RoomA	RoomB	Foyer
9:00	Opening Remarks, Conference Outline, Program Schedule		
9:10	**Tutorial Speech 1** **Prof. Christophe Vallée/CNSE**		
9:40	Break		
9:45	**Tutorial Speech 2** **Prof. Yasuteru Shigeta/University of Tsukuba**		
10:15	Break		
10:20	**Tutorial Speech 3** **Dr. Tatsuhiko Higashiki/Kioxia**		
10:50	Break		
11:00	**Keynote Speech 1** **H.E. Mr. Sibi George/Ambassador of India to Japan**		
11:15	Break		Exhibition 11:15-18:30
11:30	**Keynote Speech 2** **Mr. Hidemichi Shimizu/METI**		
12:10	**Sponsor Exhibition, Lunch Break**		
13:20	**Keynote Speech 3** **Dr. Daisuke Okanohara /Preferred Networks**		
14:00	Break		
14:10	**MC-044** Hsin-Tzu Hsu, National Taiwan University	**PO-014** Miyuki Kouda, Kioxia	
14:30	**MC-028** Yurika Suzuki, University of Tsukuba	**PO-023** Shigeru Kinoshita, Kioxia	
14:50	**MC-026** Young Jae JANG, KAIST	**PO-007** Akira Uedono, University of Tsukuba	
15:10		**PO-021** Kiyoteru Kobayashi, ESCO	
15:30	**Authors' Inteview, Exhibition, & Break**		
15:50	ONLINE <Invited> EDTM-215 Prof. Hitoshi Wakabayashi, Institute of Science Tokyo	<Invited> EDTM-496 Prof. Shin-ichi Nishizawa, Kyushu University	
16:10	<Invited> **PC-042** Prof. Makoto Sekine, Nagoya University	**PO-032** Keisuke Miyamoto, TOSHIBA ELECTRONIC DEVICES & STORAGE	
16:30	**PC-039** Kazuki Yanagita, INFICON	**PO-019** Katsumi Rikimaru, TOSHIBA ELECTRONIC DEVICES & STORAGE	
16:50	**Authors' Inteview, Exhibition, & Break**		
17:10	**PC-034** Kuan-Chun Lin, National Taiwan University	**PO-046** KANGBAI LI, Institute of Science Tokyo	
17:30	**PC-010** Koichi Sumiya, University of Tsukuba	**PO-024** Kyohei Matsumoto, Hiroshima University	
17:50	**PC-017** Anthony Vasquez, INFICON	**PO-029** Hiroya Iwashiro, GlobalWafers Japan	
18:10	**Authors' Inteview, Exhibition, & Break**		
18:30 – 20:00	**Reception**		

December 10 (Day-2)

JST(UTC+9)	RoomA	RoomB	Foyer
9:00	Program Outline		Exhibition 9:00-14:00
9:10	**Keynote Speech 4** **Dr. Takeshi Nogami/IBM Research**		
9:50	Break		
10:00	**Keynote Speech 5** **Dr. Katsuya Oguri/NTT Basic Research Laboratories**		
10:40	Break		
10:50	**Keynote Speech 6** **Dr.Yasuhiro Morikawa/ULVAC**		
11:30	**Flash Presentation by Poster Authors** PO-008 : Tsubasa Kobayashi, Kogakuin University PO-011 : Hironori Chatani, ULVAC ES-012 : Toshiya Soyama, ULVAC PO-031 : Kento Moriya, Kogakuin University PO-038 : Shinri Yamadera, Kogakuin University PO-040 : Kanta Kibishi, Kogakuin University		
12:00	**Poster Session, Sponsor Exhibition, & Lunch Break**		
13:00	**Special Session** **Prof. Tadahiro Kuroda/The University of Tokyo**		
13:50	Break		
14:00	ONLINE <Invited> IITC-11.5 **V.M. Blanco Carballo, IMEC**	ONLINE <Invited> EDTM-470 Prof. Junichi Koike, Tohoku University	
14:20	**YE-013** Kazuto Kawakatsu, Sony Semiconductor Solutions	**PC-015** Masaaki Takada, Toshiba	
14:40	ONLINE <Invited> IITC-11.4 **Karine Abadie, CEA-Leti**	**PC-009** Kazuya Kikuchi, TOSHIBA ELECTRONIC DEVICES & STORAGE	
15:00	**Authors' Inteview & Break**		
15:20	**YE-018** **Kyohei Tsutano, ORGANO**	**PC-043** Christian Milleneuve Budiono, The University of Tokyo	
15:40	**YE-033** **Yutaka Sawai, Rohm**	**PC-030** Ryosuke Okachi, Toyota Central R&D Labs	
16:00	**YE-022** Kenta Horide, SCREEN Advanced System Solutions	**PC-037** Tatsuya Watanabe, Sony Semiconductor Manufacturing	
16:20	**Authors' Inteview & Break**		
16:40	**MC-045** Jakey Blue, National Taiwan University	**ID-035** Kenji Kanda, Mie University	
17:00	**DM-020** **Atsuko Enomoto, Hitachi**	**ID-036** Chieh-Yu Chen, National Taiwan University	
17:20		**ID-025** Tori Wright, University of Central Florida	
17:40	**Authors' Inteview & Break**		
18:00	**Best Paper&Student Awards,** **Farewell Party**		

MC: Manufacturing Control and Execution
PO: Process/Material Optimization
PC: Process Monitoring and Control Method
YE: Yield Enhancement and Methodology
DM: Design for Manufacturing
ID: Intelligent Data Management
IITC: Invited papers from IEEE International Interconnect Technology Conference (IITC) 2024
EDTM: Invited papers from IEEE Electron Device Technology and Manufacturing Conference (EDTM)2024

Message from ISSM 2024 Committee

Shozo Saito
Chairman of Organizing Committee of ISSM 2024
Representative Director & Chairman
Nippon Electronic Device Industry Association (NEDIA)

On behalf of the organizing committee, it is my great pleasure to extend to you all a very warm welcome to the International Symposium on Semiconductor Manufacturing (ISSM) 2024. ISSM is a premier conference for semiconductor manufacturing professionals dedicated to sharing technical solutions and opinions on the advancement of manufacturing science, technologies, and management disciplines. Since its start in 1992 in Japan, ISSM has been providing unique opportunities to share semiconductor manufacturing technology," best practices" for the benefit of professionals worldwide.

ISSM aims to establish new concepts for semiconductor manufacturing technologies and to promote them as systemized and universalized technologies. ISSM brings together researchers and engineers involved in semiconductor manufacturing technology from a wide range of industries and universities. This year, ISSM will celebrates its 30th anniversary.

Looking at the global semiconductor industry, the growth momentum is expected to continue in the long range, and it is expected to exceed 100 trillion yen by 2025. Especially, the rise of generative AI applications, such as ChatGPT and Copilot, has led to a surge in demand for computational power. This translates to higher demand for semiconductors, pushing the industry to innovate faster and produce more capable and efficient chips. On the other hand, what about the semiconductor industry in Japan? In the past, Japan's technological capabilities and innovation stood out and led the world. However, the last 20 years have been challenging, and the share of semiconductor production in Japan last year was 8%. However, the wind direction is about to change 180 degrees. This is because semiconductors have begun to be recognized as highly important for ensuring stability in terms of economic security. In particular, advanced semiconductors are an important strategic commodity, and countries around the world are increasingly strengthening their own development and production. This change should not be seen as a mere temporary increase in demand, but as the beginning of a major transformation that will fundamentally change the way the semiconductor supply chain works. Japan will work together with the public and private sectors, including large-scale subsidies, to attract TSMC to Kumamoto, support for domestic semiconductor manufacturers including Micron, establish Rapidus. We are trying to breathe new life into semiconductor manufacturing in Japan. While these developments open up new possibilities for the semiconductor industry, the 20-year gap also presents significant challenges. Now, as experts in semiconductor production technology, we would like to sort out these issues and use this as a forum for discussions to open up the future for strengthening and rebuilding the domestic semiconductor manufacturing base from the perspective of production technology. We will continue to work together with the industry to develop semiconductor manufacturing technology.

Today we are together here at ISSM to reaffirm the key role that semiconductor manufacturing and its environment throughout the supply chain, in ensuring our industry's ongoing progress. Besides the series of technical papers from all over the world, we are honor to have 6 marvelous keynote and invited speakers, and 3 tutorial speakers ISSM has been collaborating with global affiliation including Taiwan Semiconductor Industry Association (TSIA), SEMI, SEAJ, Minimal Fab Promotion Organization (MINIMAL). I would like to express our special appreciation to our partner, ISSM is an excellent opportunity to make connections and explore new collaborations, as we share ideas and perspectives on challenges and opportunities in both technology and manufacturing. I would like to express my deepest gratitude to the sponsored companies, and to all the committee members involved in organizing this symposium. Finally, I offer my best wishes for highly productive information exchange among everyone at ISSM 2024.

Dr. Ayako Shimazaki

Chairman of Executive Committee of ISSM 2024

Technology Executive

Toshiba Nanoanalysis Corporation

On behalf of the ISSM 2024 Executive Committee, I would like to thank all of you for your participation in the 30th ISSM 2024.

For the last couple of years, Artificial Intelligence (AI) has been leading the growth of the global semiconductor industry and still AI promises to impact the growth of semiconductor market for years to come as a core driving factor of transformative applications among end-markets.

The ISSM will celebrate its 30th anniversary featuring keynotes and global industry leaders sharing the outlook of dynamic emerging market, analysis of global semiconductor market, and advanced technology trends.

His Excellency Sibi George, Ambassador of India to Japan demonstrates its significance as a platform for the global semiconductor industry. Mr. Hidemichi Shimizu of Ministry of Economy, Trade and Industry will highlight Japan's "Semiconductor and Digital Industry Strategy" to accelerate the advanced semiconductor technologies including the advanced packaging technology and other production and manufacturing technologies. Dr. Daisuke Okanohara of Preferred Networks will discuss the integration of AI and semiconductor manufacturing and challenges of semiconductor for realizing AI in the future. Dr. Takeshi Nogami of IBM Research will cover 2nm node interconnect technology and R&D toward 1.4nm node and beyond aiming to revive Japan's semiconductor technology. Dr. Katsuya Oguri of NTT Basic Research Laboratories will introduce R&D activities of the Innovative Optical and Wireless Network (IOWN), a next-generation telecommunications infrastructure initiative and a further future beyond. Dr. Yasuhiro Morikawa of ULVAC will address highly accurate via formation technologies for advanced -packaging process using plasma dry etching aiming to achieve both high energy efficiency and low-latency real-time processing.

From our partner conference, EDTM and IITC, we are honor to have five invited talks.

We invited three tutorial speakers. Prof. Christophe Vallée of University at Albany, CNSE, will cover 50 years of thin film processing innovation in SC industry and how they now combine to open the door to new concepts that facilitate integration, such as selective deposition. Prof. Yasuteru Shigeta of University of Tsukuba will discuss computational materials science studies on the search for potential dopant candidates. Dr. Tatsuhiko Higashiki of Kioxia will provide insights into the evolution of semiconductor lithography and the innovative solutions being developed to address the challenges of the future.

As a special session, we invited Prof. Tadahiro Kuroda, the University of Tokyo to address the challenging issues the semiconductor industry has been facing with including how to develop human resources for the next generation, as well as the establishment of an educational system for the development of semiconductor human resources. Prof. Kuroda's special speech will be followed by the panel discussion on human resources in the semiconductor Industry.

I hope that the participants of ISSM 2024 evaluate the outlook of ISSM committee for preparation of change in this industry.

Dr. Shin-ichi Imai
Chairman
Program Committee of ISSM2024
Hitachi High-Tech Corporation

Welcome to the 30th International Symposium on Semiconductor Manufacturing (ISSM) 2024.

ISSM aims to "design the future semiconductor manufacturing," and will boldly embrace the movement of new changes in semiconductor manufacturing and lead the innovative technologies in semiconductor production more than ever before.

Currently, there are dramatical changes in terms of economic security internationally, such as the restructure of the supply chain of cutting-edge logic semiconductor chips and the emergence of a foundry by a foundry. Under international cooperation, new factories are being actively constructed in Japan and other countries around the world. In order to realize the miniaturization of transistors with a secure operating margin, research and development are progressing on new device physics and the introduction of new materials are advancing. With the time-to-market supply of AI chips as a competitive advantage in the market, a new challenge to ultra-short TAT production is garnering attention. The transition from conventional semiconductor manufacturing mixed batch and wafer processes to full single-wafer manufacturing has become a hot topic, and the adoption of latest trends and innovative technologies, such as 3D package, chiplet integration and their manufacturing technologies, are also urgently needed.

ISSM Program Committee consisted by 25 members from 24 affiliations including semiconductor device, equipment and materials manufacturers, revised the areas of the interests and highlighted themes for ISSM 2024 through intimate discussion among members. ISSM 2024 highlights IoT and AI Solution, Next Generation Fab, Sustainable Manufacturing and Promotion of Global Environmental Conservation and 3D Packaging and Chiplet Integration: New Horizon from Integration to Testing.

ISSM 2024 has received an abundance of high-quality abstracts full of insight and useful know-hows. Through tough review process by Program Committee members, 36 papers were selected including 14 papers for Process/Material Optimization (PO) , 10 papers for Intelligent Data Management (PC), followed by 4 papers for Process Monitoring & Control Method (MC), 4 papers for Yield & Defect Control (YE), 3 papers for Manufacturing Strategy (ID) And 1paper for Fab Operation Method (DM) and Environment, Safety and Health, Carbon Neutral (ES). We will also feature 6 keynote speeches by world-renowned industry experts, focusing on topics relevant for today's economic and manufacturing climate. Also 3 tutorial sessions focused on covering a well-defined topic will take place in the morning of the first day. And also 6 invited talks from cooperative conferences, EDTM, IITC and Nagoya University.

I would like to extend my sincere appreciation to all authors and speakers, sponsors, committee members, moderators, and, last but not least, all the participants. I hope you will enjoy the technical program of ISSM 2024, take this opportunity to network with experts around the world, and bring back good memories with you.

Keynote Speakers

Monday, December 9

Semiconductor Ecosystem : India-Japan Strategic Partnership

His Excellency Sibi George
Ambassador of India to Japan

Japan's semiconductor strategy

Hidemichi Shimizu
Director of Device Industry & Semiconductor Strategy Office, Commerce and Information on Policy Bureau, Ministry of Economy, Trade and Industry

AI and Semiconductor Manufacturing – opportunities and challenges

Dr. Daisuke Okanohara
Chief Executive Researcher
Preferred Networks, Inc.

Tuesday, December 10

2nm Node Interconnect Technology and R&D toward 1.4nm Node and Beyond

Dr. Takeshi Nogami
Principal Research Staff Member,
Lead Technologist / Strategist for BEOL Extendibility
IBM Research

Research and development in NTT Basic Research Laboratories towards IOWN and beyond

Dr. Katsuya Oguri
NTT Basic Research Laboratories

Highly Accurate Via Formation Technologies for Advanced Packaging Process Using Plasma Dry Etching

Dr. Yasuhiro Morikawa

Manager, PE-Semiconductor Technology Research Department Institute of Advanced Technology, Research & Development HQ

ULVAC, Inc.

Tutorial Speakers

Monday, December 9

50 years of thin film processing innovation in SC industry

Prof. Christophe Vallée

Professor, University at Albany, CNSE

Computational materials science studies on the search for potential dopant candidates.

Prof. Yasuteru Shigeta

Vice president and Executive Director for Research

Professor of Center for Computational Sciences

University of Tsukuba

The History and Future of Semiconductor Lithography: New Prospects Beyond the Limits of Pattern Shrinking

Dr. Tatsuhiko Higashiki

Assistant to General Manager, Research Strategy Planning Office, Frontier Technology R&D Institute, Kioxia

Japanese to English simultaneous interpretation will be available ONLY for Tutorial Sessions.

Special Session Speaker

Tuesday, December 10

Improving energy efficiency and development efficiency

Prof. Tadahiro Kuroda

University Professor, Office of University Professor, The University of Tokyo

Chancellor, Prefectural University of Kumamoto

Symposium Schedule (Day-1)

ISSM2024
Monday, December 9, 2024

Room: KFC Hall

8:30	Registration Open
9:00-9:10	**Opening** **Opening Remarks** Shozo Saito, Chairman of Organizing Committee of ISSM2024 **Conference Outline** Ayako Shimazaki, Chairman of Executive Committee of ISSM2024 **Program Outline** Shin-ichi Imai,, Chairman of Program Committee of ISSM2024 MC: Shuichi Inoue, Vice Chairman of Organizing Committee of ISSM2024
9:10- 9:40	**Tutorial Speech-1** **50 years of thin film processing innovation in SC industry** Prof. Christophe Vallée, University at Albany, CNSE Session Chair: Tsuyoshi Moriya, Tokyo Electron
9:40- 9:45	Break
9:45-10:15	**Tutorial Speech-2** **Computational materials science studies on the search for potential dopant candidates.** Prof. Yasuteru Shigeta, University of Tsukuba Session Chair: Tsuyoshi Moriya, Tokyo Electron
10:15-10:20	Break
10:20-10:50	**Tutorial Speech-3** **The History and Future of Semiconductor Lithography: New Prospects Beyond the Limits of Pattern Shrinking** Dr. Tatsuhiko Higashiki, Kioxia Session Chair: Ayako Shimazaki, Toshiba Nanoanalysis
10:50-11:00	Break
11:00-11:15	**Keynote Speech-1** **Semiconductor Ecosystem : India-Japan Strategic Partnership** H.E. Mr. Sibi George, Ambassador of India to Japan Session Chair: Shozo Saito, Nippon Electronic Device Industry Association (NEDIA)
11:15-11:30	Break and Platinum Sponsor ‘s Video
11:30-12:10	**Keynote Speech-2** **Japan’s semiconductor strategy** Hidemichi Shimizu, Ministry of Economy, Trade and Industry Session Chair: Hiroshi Akahori, Rapidus
12:10-13:20	Sponsor Exhibition / Lunch Break
13:20-14:00	**Keynote Speech-3** **AI and Semiconductor Manufacturing – opportunities and challenges** Dr. Daisuke Okanohara, Preferred Networks, Inc. Session Chair: Tsuyoshi Moriya, Tokyo Electron
14:00-14:10	Break

Symposium Schedule (Day-1)

Room1: KFC Hall

Session A-1 : Manufacturing Control and Execution (MC)
Session Co-chairs: Hiroyuki Inoue, Texas Instruments Japan / Minoru Inomoto, KIOXIA

14:10	**MC-044 : Deep Reinforcement Learning-based Effective Training Design for Dynamic Machine Allocation with Case Study of a Semiconductor Tool Group** Hsin-Tzu Hsu, National Taiwan University
14:30	**MC-028 : Multi-factory scheduling considering the trade-offs between production efficiency and risks** Yurika Suzuki, University of Tsukuba
14:50	**MC-026 : AI and Digital Twin Integration in Autonomous Robot Orchestration Solution (AROS)** Young Jae JANG, KAIST
15:10	<Withdraw>
15:30	Author's Interview & Exhibition (On-Site ONLY)& Break

Session A-2: EDTM&Process Monitoring and Control Method (PC)
Session Co-Chairs: Shin-ichi Imai, Hitachi High-Tech / Satoko Nakagawa, GlobalWafers Japan

15:50	ONLINE **<INVITED>EDTM-215 : Reduction of contact resistance to PVD-MoS2 film using aluminum–scandium alloy (AlSc) edge contact** Prof. Hitoshi Wakabayashi, Institute of Science Tokyo
16:10	**<INVITED>PC-042 : Understanding Surface Reaction in PECVD Process by Combining In-situ Monitoring and Machine Learning** Makoto Sekine, Nagoya University
16:30	**PC-039 : Novel Optical Gas Analyzers based on Self-Plasma Optical Emission Spectroscopy and their applications in Semiconductor Manufacturing** Kazuki Yanagita, INFICON
16:50	Author's Interview (On-Site ONLY) & Break

Session A-3: Process Monitoring and Control Method (PC)
Session Co-Chairs: Masami Aoki, KLA-Tencor Japan / Takayuki Matsumoto, United Semiconductor Japan

17:10	**PC-034 : Proactive Control Setting of Real Time Equipment Monitoring for Raising End-of-Line Process Performance** Kuan-Chun Lin, National Taiwan University
17:30	**PC-010 : Classification of Multivariate Time Series Signals Using Self-Supervised Representation Learning for Condition Monitoring** Koichi Sumiya, University of Tsukuba
17:50	**PC-017 : AI/ML Deployment at the Edge for Run-by-Run and Real-Time Analysis** Anthony Vasquez, INFICON
18:10	Author's Interview (On-Site ONLY) & Break
18:30 – 20:00	Reception

Room 2: KFC Hall Annex

Session B-1 : Process/Material Optimization (PO)
Session Co-chairs: Isamu Namose, OMRON / Toshio Konishi, Tekscend Photomask

14:10	**PO-014 : Optimal Design of Wet Etching Bath for 3D Flash Memories Using Multi-Objective Bayesian Optimization** Miyuki Kouda, Kioxia
14:30	**PO-023 : Space-filling experimental design for efficient Bayesian optimization** Shigeru Kinoshita, Kioxia
14:50	**PO-007 : Vacancy-type defects in thin HfO2 layers probed by monoenergetic positron beams** Akira Uedono, University of Tsukuba
15:10	**PO-021 : Characterization of Hydrogen Desorption and Charge Traps in Silicon Nitride Films** Kiyoteru Kobayashi, ESCO, Ltd.
15:30	Author's Interview & Exhibition (On-Site ONLY)& Break

Session B-2: EDTM& Process/Material Optimization (PO)
Session Co-Chairs: Shinsuke Mizuno, Applied Materials Japan / Ayako Shimazaki, Toshiba Nanoanalysis

15:50	**<INVITED>EDTM-496 : SiC Materials and Devices for Future Green Society** Prof. Shin-ichi Nishizawa, Kyushu University
16:10	**PO-032 : Improvement of P-base contact resistance in power MOSFETs and its impact on avalanche capability** Keisuke Miyamoto, TOSHIBA ELECTRONIC DEVICES & STORAGE
16:30	**PO-019 : Avalanche Capability Improvement by Ion Implantation-induced Defects Control for Trench Power MOSFET** Katsumi Rikimaru, TOSHIBA ELECTRONIC DEVICES & STORAGE
16:50	Author's Interview (On-Site ONLY) & Break

Session B-3: Process/Material Optimization (PO)
Session Co-Chairs: Shun-ichiro Ohmi, Institute of Science Tokyo / Yuki Yamada, JX Advanced Metals

17:10	**PO-046 : Ar/N2 gas flow rate dependence on the ferroelectric HfN1.15 thin film formation by ECR-plasma sputtering** KANGBAI LI, Institute of Science Tokyo
17:30	**PO-024 : Investigation on the Relationship Etching Rate and Photoresist Surface Temperature during Reactive Atmospheric-pressure Thermal Plasma Jet Irradiation** Kyohei Matsumoto, Hiroshima University
17:50	**PO-029 : First-Principles Analysis for Estimating the Gettering Effects of Vacancy–Oxygen Complexes (VOx) in Rapid Thermal Processing Wafers** Hiroya Iwashiro, GlobalWafers Japan
18:10	Author's Interview (On-Site ONLY) & Break
18:30 – 20:00	Reception

Symposium Schedule (Day-2)

ISSM2024
Tuesday, December 10, 2024

Room: KFC Hall

8:30 Registration Open

9:00-9:10 **Program Outline**
Shin-ichi Imai,, Chairman of Program Committee of ISSM2024
MC: Shuichi Inoue, Vice Chairman of Organizing Committee of ISSM2024

9:10- 9:50 **Keynote Speech-4**
2nm Node Interconnect Technology and R&D toward 1.4nm Node and Beyond
Dr. Takeshi Nogami, IBM Research
Session Chair: Katsutoshi Ozawa, OMRON

9:50-10:00 Break

10:00-10:40 **Keynote Speech-5**
Research and development in NTT Basic Research Laboratories towards IOWN and beyond
Dr. Katsuya Oguri, NTT
Session Chair: Shun-ichiro Ohmi, Institute of Science Tokyo

10:40-10:50 Break

10:50-11:30 **Keynote Speech-6**
Highly Accurate Via Formation Technologies for Advanced Packaging Process Using Plasma Dry Etching
Dr. Yasuhiro Morikawa, ULVAC
Session Chair: Kenji Miyake, Office Miyake

11:30-12:00 **3mins Flash Presentation by Poster Speakers**
Session Co-chairs: Minoru Inomoto, KIOXIA / Toshio Konishi, Tekscend Photomask
PO-008 : Optimization of post-deposition annealing conditions for p-type SnO fabrication by low-concentration hydrogen sputtering using SnO2 sputtering target
Tsubasa Kobayashi, Kogakuin University
PO-011 : Enhancing Process Engineering Decision-Making with Model Visualization Techniques
Hironori Chatani, ULVAC
ES-012 : A New Operational Method for Green Transformation in Semiconductor Manufacturing
Toshiya Soyama, ULVAC
PO-031 : Fabrication of SnSO4 transparent thin-films using simultaneous oxidation and sulfurization annealing
Kento Moriya, Kogakuin University
PO-038 : UV exposure in an oxygen atmosphere at room temperature as a new method for improvement of amorphous oxide TFT characteristics
Shinri Yamadera, Kogakuin University
PO-040 : Strong amorphization in In2O3-based flexible transparent conductive films by hydrogen incorporation and higher sputtering pressure
Kanta Kibishi, Kogakuin University

12:00-13:00 **Poster Session, Sponsor Exhibition & Lunch Break**

13:00-13:50 **Special Session**
Improving energy efficiency and development efficiency
Prof. Tadahiro Kuroda, The University of Tokyo
Session chair: Shuichi Inoue, ATONARP INC.

Panel Discussion organized by ISSM committee
Human resources to vitalize Japan's semiconductor industry
The short panel discussion following by the special talk by Prof. Kuroda will discuss about the critical challenges facing by the semiconductor industry.
The topics may include:
- What kind of skills do engineers need for an advanced semiconductor plant, and how can they be trained?
- What human resources are needed to weave the missing pieces for Japan's semiconductor industry”?
- How do we solve the issues?

Moderator:
Shuichi Inoue, ATONARP INC.

Panelists:
Tadahiro Kuroda, The University of Tokyo/Prefectural University of Kumamoto
Kazunori Kato, Advanced Interface Technology Corporation
Kenji Miyake, Office Miyake
Shin-ichi Imai, Hitachi High-Tech

13:50-14:00 **Break**

Symposium Schedule (Day-2)

Room1: KFC Hall

Session A-4 : IITC & Yield Enhancement and Methodology (YE)
Session Co-Chairs:Kazunori Kato, Advanced Interface Technology / Shun-ichiro Ohmi, Institute of Science Tokyo

14:00	ONLINE **<INVITED>IITC-11.5 : Bonding induced distortion in wafer-to-wafer bonding applications: how the scanner and Yieldstar can enable 3D integration** V.M. Blanco Carballo, IMEC
14:20	**YE-013 : Accuracy Improvement of Chip-on-Wafer Surface Defect Inspection by Deep Learning** Kazuto Kawakatsu, Sony Semiconductor Solutions
14:40	ONLINE **<INVITED>IITC-11.4 : Study and Control of the Distortion Induced by the Bonding Process for BSPDN Approaches** Karine Abadie, CEA-Leti
15:00	Author's Interview (ON-Site ONLY) & Break

Session A-5: Yield Enhancement and Methodology (YE)
Session Co-Chairs:Takatoshi Yasui, Tower Partners Semiconductor / Takayuki Matsumoto, United Semiconductor Japan

15:20	**YE-018 : Evaluation of Metal Contamination Behavior on Silicon Dioxide Surface Rinsed with Deionized Water Containing Ultra-trace Metal in Single-wafer Cleaning Process** Kyohei Tsutano, ORGANO
15:40	**YE-033 : Rapid and Flexible Yield Analysis Powered by Large Language Model** Yutaka Sawai, Rohm
16:00	**YE-022 : Annotation Effort Reduction for Introducing AI into Optical Inspection Systems** Kenta Horide, SCREEN Advanced System Solutions
16:20	Author's Interview (On-Site ONLY) & Break

Session A-6: Manufacturing Control and Execution (MC) & Design for Manufacturing (DM) & IITC
Session Co-Chairs: Takayuki Hisamatsu, Sony Semiconductor Manufacturing / Shinsuke Mizuno, Applied Materials Japan

16:40	**MC-045 : Predictive Equipment State Based on Hidden Markov Model and Production Plan** Jakey Blue, National Taiwan University
17:00	**DM-020 : Automatic Disassembly Standard Time Estimate System For improving Etch System Maintenance** Atsuko Enomoto, Hitachi
17:20	Author's Interview (On-Site ONLY) & Break
17:40	Break
18:00 – 18:30	Best Papers & Student Awards, Farewell Party

Room 2: KFC Hall Annex

Session B-4: EDTM & Process Monitoring and Control Method (PC)
Session Co-Chairs: Masami Aoki, KLA-Tencor Japan / Satoko Nakagawa, GlobalWafers Japan

14:00	ONLINE **<INVITED>EDTM-470 : Intermetallic compounds for future ULSI metallization** Prof. Junichi Koike, Tohoku University
14:20	**PC-015 : Virtual Metrology using Transfer Learning with Domain Knowledge** Masaaki Takada, Toshiba
14:40	**PC-009 : Quick update of Virtual Metrology using Weighted Transfer Lasso** Kazuya Kikuchi, TOSHIBA ELECTRONIC DEVICES & STORAGE
15:00	Author's Interview (ON-Site ONLY) & Break

Session B-5 : Process Monitoring and Control Method (PC)
Session Co-Chairs:Tsuyoshi Moriya, TEL / Yuki Yamada, JX Advanced Metals

15:20	**PC-043 : Fast Temperature Control in Semiconductor Vertical Furnace with Time-Optimal Control and Iterative Experiments** Christian Milleneuve Budiono, The University of Tokyo
15:40	**PC-030 : Case Study on Modeling of Multiple Process Using Intermediate Variables for Digital Twin Modeling of a Semiconductor Manufacturing** Ryosuke Okachi, Toyota Central R&D Labs., Inc.
16:00	**PC-037 : Improvement of Process Conditions using Hierarchical Optimization** Tatsuya Watanabe, Sony Semiconductor Manufacturing
16:20	Author's Interview (On-Site ONLY) & Break

Session B-6 : Intelligent Data Management (ID)
Session Co-Chairs: Kazuhito Matsukawa, SUMCO / Hiroyuki Inoue, Texas Instruments Japan

16:40	**ID-035 : Classifiers and Clustering Based Approach for Imbalanced Wafer Map Data** Kenji Kanda, Mie University
17:00	**ID-036 : Unsupervised and Spectral Feature-based Sensor Relation Identification for Advanced Equipment Anomaly Detection** Chieh-Yu Chen, National Taiwan University
17:20	**ID-025 : Generalized vs. Individualized Kaplan-Meier Time-to-Failure Predictive Models for Preventative Maintenance in Semiconductor Manufacturing** Tori Wright, University of Central Florida
17:40	Author's Interview (On-Site ONLY) & Break
18:00 – 18:30	Best Papers & Student Awards, Farewell Party

Symposium Schedule (Day-2)

ISSM2024

Tuesday, December 10, 2024

Interactive Poster Session

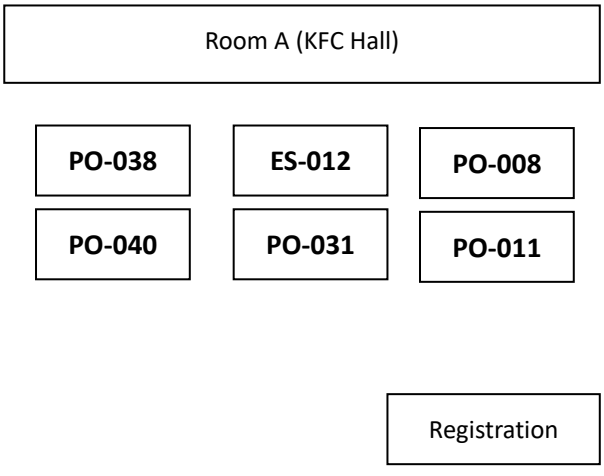
11:30-12:00 3-min Flash Presentation for Interactive Poster Session @ Room A : KFC Hall

Session Co-chairs: Minoru Inomoto, KIOXIA / Toshio Konishi, Tekscend Photomask

PO-008 : Optimization of post-deposition annealing conditions for p-type SnO fabrication by low-concentration hydrogen sputtering using SnO2 sputtering target Tsubasa Kobayashi, Kogakuin University
PO-011 : Enhancing Process Engineering Decision-Making with Model Visualization Techniques Hironori Chatani, ULVAC
ES-012 : A New Operational Method for Green Transformation in Semiconductor Manufacturing Toshiya Soyama, ULVAC
PO-031 : Fabrication of SnSO4 transparent thin-films using simultaneous oxidation and sulfurization annealing Kento Moriya, Kogakuin University
PO-038 : UV exposure in an oxygen atmosphere at room temperature as a new method for improvement of amorphous oxide TFT characteristics Shinri Yamadera, Kogakuin University
PO-040 : Strong amorphization in In2O3-based flexible transparent conductive films by hydrogen incorporation and higher sputtering pressure Kanta Kibishi, Kogakuin University

12:00-13:00 Poster Session @ Foyer

Poster Layout



Abstracts of technical papers

Session A-1

MC-044 Deep Reinforcement Learning-based Effective Training Design for Dynamic Machine Allocation with Case Study of a Semiconductor Tool Group Hsin-Tzu Hsu, National Taiwan University

Dynamic Machine Allocation (DMA) is crucial in semiconductor production scheduling. Current production lines rely heavily on engineers' experience, but during unfamiliar economic transitions, manual DMA adjustments take 2-3 days, making rapid response to line changes difficult and leading to throughput deviations and backorders. To address this, we introduce a novel Deep Reinforcement Learning (DRL)-based DMA design to reduce reliance on expertise and improve policy update speed. Key innovations include a two-stage DRL and optimization integration, plus a Neural Network (NN) output transformation module to enforce operational constraints. Simulation using real fab data on a metal sputtering tool group shows our approach learns new policies in about 1 hour, outperforming heuristic methods by 3-20% in various scenarios.

MC-028 Multi-factory scheduling considering the trade-offs between production efficiency and risks
Yurika Suzuki, University of Tsukuba

Parallel decentralized production, in which multiple factories share production sorts, is on the rise to achieve a stable supply. We propose multi-factory and multi-objective production scheduling with resource allocation to improve multiple metrics such as quality throughput, setup time, and Q-time compliance rate. First, proposed P3D-QAP2MF of a machine allocation algorithm beyond factories is verified. Second is to integrate it with a multi-objective multi-factory hybrid flow-shop scheduling DABC-TRANS method based on DABC (a discrete artificial bee colony) and to verify those synergistic effect. Compared to Critical Ratio-based conventional method, P3D-QAP2MF improves rates of Q-time compliance, on-time delivery and setup time. Furthermore, the algorithm that combines P3D-QAP2MF and DABC-TRANS achieve highly performance than P3D-QAP2MF in terms of on-time delivery and setup time. Our proposal can achieve improvements of production efficiency and risk distribution in Multi-factory.

MC-026 AI and Digital Twin Integration in Autonomous Robot Orchestration Solution (AROS) Young Jae JANG, KAIST The Autonomous Robot Orchestration Solution (AROS) advances manufacturing automation by revolutionizing large-scale robotic fleet management. AROS monitors robot states and their environment, enabling autonomous collaboration in semiconductor fabrication facilities, specifically for Overhead Hoist Transport (OHT) operations. The system combines reinforcement learning for decision-making with deep auto-encoder models for monitoring, enhanced by Digital Twin technology for real-time simulation-based optimization. Implementation in operational facilities demonstrates significant improvements in delivery efficiency and capacity, with autonomous anomaly detection reducing human intervention. Our results, validated in large-scale semiconductor manufacturing, establish AROS as a pioneering solution for autonomous factory operations.

Session A-2

PC-039 Novel Optical Gas Analyzers based on Self-Plasma Optical Emission Spectroscopy and their applications in Semiconductor Manufacturing Huidong Zang, INFICON

The novel sensor for Leak detection, using Self-Plasma OES. This SP-OES can be used at dark chambers and even other dark locations. By using this sensor for Real time leak detection of metallization process, high ROI can be archived by preventing wafer scraps.

Session A-3

PC-034 Proactive Control Setting of Real Time Equipment Monitoring for Raising End-of-Line Process Performance
Kuan-Chun Lin, National Taiwan University

End-of-Line (EOL) process performance can be significantly influenced by the stability of equipment processes. Real-time monitoring serves as a crucial measure for tracking equipment process conditions. Proactively controlling real-time monitoring during in-line processing is essential for enhancing end-of-line wafer quality. We present an innovative design with three key components: selection of critical real-time equipment monitoring (RTM) items, prediction of wafer acceptance test (WAT) parameters, and optimization of RTM control parameter settings. Experimental results demonstrate that our proactive control design outperforms three commonly used methods by industry or for numerical target prediction. Additionally, we illustrate how RTM control settings may impact the outcome of a WAT parameter.

Keywords—machine learning, semiconductor manufacturing, wafer acceptance test, equipment sensory data, equipment monitoring optimization, genetic algorithm."

PC-010 Classification of Multivariate Time Series Signals Using Self-Supervised Representation Learning for Condition Monitoring Koichi Sumiya, University of Tsukuba

In the analysis of real-world data, two significant challenges often arise: high-dimensional signals and their temporal interactions. To address these issues and identify transitions in process conditions through end-to-end learning, we propose a self-supervised representation learning framework that conceptualizes signals as images. This straightforward approach classifies imaged signals as time-specific conditions by maximizing mutual information within a domain-specific feature space. We applied this methodology to two labeled open datasets and one unlabeled real-world process dataset, yielding promising results.

PC-017 AI/ML Deployment at the Edge for Run-by-Run and Real-Time Analysis Anthony Vasquez, INFICON
As semiconductor manufacturing advances to smaller technology nodes, achieving high yield demands precise, stable processes supported by advanced sensors and responsive control systems. Conventional AI/ML model deployment on a central server limits time-sensitive applications critical for real-time and run-by-run (RbR) fault detection and control (FDC). This paper introduces a system for deploying AI/ML models at the edge, integrating the low-latency Libtorch library with INFICON's FabGuard. This design facilitates real-time analysis, enhances FDC capabilities, and enables seamless integration of user-developed models without requiring additional MLOps infrastructure. We demonstrate the system's utility through two applications.

Session A-4

YE-013 Accuracy Improvement of Chip-on-Wafer Surface Defect Inspection by Deep Learning Kazuto Kawakatsu, Sony Semiconductor Solutions Surface defect inspection at high sensitivity is essential to ensure the quality of the Chip on Wafer (CoW) process, but a high accuracy and efficient detection of very small defects on diced and sorted chips is more difficult than that for a whole wafer, owing the presence of specific false defects. In this study, we aimed to reduce the detection rate of false defects and detect only target defects, by applying automatic image classification using Deep Learning.

Session A-5

YE-018 Evaluation of Metal Contamination Behavior on Silicon Dioxide Surface Rinsed with Deionized Water Containing Ultra-trace Metal in Single-wafer Cleaning Process Kyohei Tsutano, ORGANO
The metal management value of deionized water (DIW) is required at the pg/L-level for advanced device manufacturing. However, previous studies on metallic contamination proved insufficient owing to their utilization of highly concentrated solutions at the μg/L-level. In this study, we investigated the contamination behavior of metal impurities at the pg/L-level in DIW on the SiO2 surface using a single-wafer cleaning process. The SiO2 surface concentration of Al, Ti, Fe, Zn, and Ga linearly increased with both the concentration in DIW increased and the rinse time, while it was constant with supply flow rate of DIW. We assumed that the adsorption probability decreased owing to the reduction of the metal concentration in the boundary layer, which became thinner with increased supply flow rates. Herein, we provide new insights into the pertinence of both reducing metal concentrations in DIW and optimizing rinse process parameters with a single-wafer cleaning process.

YE-033 Rapid and Flexible Yield Analysis Powered by Large Language Model Yutaka Sawai, Rohm
Semiconductor manufacturing involves complex processes, making yield analysis challenging for engineers. This study introduces a framework for identifying factors affecting specific characteristics using simplified descriptions, e.g., "a product's characteristic declined during a period." The framework includes four layers: input, selection, analysis, and interpretation, with key innovations in selection and interpretation. The selection layer uses large language models (LLM) to infer column attributes from metadata, enabling accurate column selection for filtering and target identification. The interpretation layer combines process details with correlation results to propose process improvements or assess risks based on semiconductor engineering principles. This approach shows the potential of integrating LLM with domain-specific methods to improve yield analysis and interpret production data effectively.

YE-022 Annotation Effort Reduction for Introducing AI into Optical Inspection Systems
Kenta Horide, SCREEN Advanced System Solutions
Optical wafer inspection equipment featuring rule-based inspection criteria is widely used in semiconductor manufacturing. Recently, we have seen an increasing movement to introduce AI, especially deep learning, to improve optical inspection. On the other hand, deep learning requires a large amount of training data, and creating the training data requires highly accurate labeling (annotation) of images. This enormous amount of effort required for annotation has been an obstacle to the introduction of AI. In this study, we have developed a method to significantly reduce the annotation effort for classification based on semi-supervised learning. We have managed to reduce annotation effort by 62–97% for a semiconductor wafer dataset with two classes, “defects” and “false defects.”

Session A-6

MC-045 Predictive Equipment State Based on Hidden Markov Model and Production Plan
Jakey Blue, National Taiwan University
This research introduces the Predictive Equipment Health Monitoring using Hidden Markov Models and Production Scheduling (PEHMM) framework to address limitations in traditional equipment health estimation. Relying on Gaussian Mixture Hidden Markov Models (GM-HMM), PEHMM operates in two phases: offline learning, which uses historical data to model equipment behavior unsupervised, and online prognostics for real-time health predictions, even without sensor data. Tested on bearing systems and Ion Mill Etching (IME) systems, the framework demonstrated effectiveness in predicting equipment health using MES and FDC data, surpassing conventional virtual metrology approaches. By leveraging Hotelling T^2 decomposition for feature analysis, PEHMM enhances decision-making in lot scheduling, equipment utilization, and yield monitoring, offering a robust tool for advanced process control (APC).

DM-020 Automatic Disassembly Standard Time Estimate System For improving Etch System Maintenance
Atsuko Enomoto, Hitachi
We propose an automatic disassembly standard time estimate system for etch system maintenance process that estimates ergonomics with a simple human kinematic model automatically postured for disassembly operations in the 3D computer graphic space.

Session B-1

PO-014 Optimal Design of Wet Etching Bath for 3D Flash Memories Using Multi-Objective Bayesian Optimization
Miyuki Kouda, Kioxia
This study introduces an innovative method utilizing Multi-Objective Bayesian Optimization (MOBO) to derive optimal wet etching bath design parameters, informed by image and physical quantity data from fluid dynamics simulations. Our approach, validated through simulation experiments, effectively identifies the best possible wet etching bath designs

YE-023 Space-filling experimental design for efficient Bayesian optimization Shigeru Kinoshita, Kioxia
In this study, we propose a space-filling Latin hypercube design with small fill distance and large separation radius based on simulated annealing for efficient Bayesian optimization. Through an example focused on optimizing high aspect ratio hole etching, we demonstrate that initial sampling with the proposed design is advantageous compared to conventional designs in terms of the convergence of Bayesian optimization with fewer experiments.

PO-007 Vacancy-type defects in thin HfO2 layers probed by monoenergetic positron beams
Akira Uedono, University of Tsukuba
Behaviors of vacancies during the amorphous-to-crystalline transition of thin HfO2 layers were studied by monoenergetic positron beams. The HfO2 layers with 4–30 nm thickness were fabricated on TiN/Si templates by atomic layer deposition technique. The major vacancy-type defects in the layers were identified as (i) Hf vacancies (VHf) coupled with oxygen vacancies (VOs) and (ii) vacancy clusters. After annealing at 500°C, the concentration of vacancy clusters increased, which was attributed to the agglomeration of intrinsic open spaces in the amorphous phase upon the phase transition from amorphous to crystalline phases. The phase transition started near the interface between the HfO2 layer and bottom electrodes (TiN). After the crystallization, the concentration of vacancy clusters decreased as the annealing temperature increased.

PO-021 Characterization of Hydrogen Desorption and Charge Traps in Silicon Nitride Films
Kiyoteru Kobayashi, ESCO, Ltd.
The hydrogen desorption during high-temperature thermal annealing from a silicon nitride film grown using a low-pressure chemical vapor deposition technique has been analyzed using thermal desorption spectroscopy. A desorption peak attributed to hydrogen released from the bulk of the nitride film appeared at 885 °C under a heating rate of 10 °C/min. The influence of high-temperature annealing on the density and the energy depth of trap states for electrons in the nitride film has also been investigated. The annealing at 950 °C resulted in a substantial decrease in trapped electron density. The energy depth of the trap states for electrons remaining after annealing was slightly deeper compared to before annealing. We suggest that changes in atomic structure accompanied by hydrogen desorption led to the reduction in the density and the change of energy depth of trap states for electrons.

Session B-2

PO-032 Improvement of P-base contact resistance in power MOSFETs and its impact on avalanche capability Keisuke Miyamoto, TOSHIBA ELECTRONIC DEVICES & STORAGE Power MOSFETs may be subjected to voltages above their maximum rated voltage under certain conditions. The maximum current that can be tolerated in such cases is called avalanche capability and is specified and guaranteed in the data sheet. Making it difficult for the parasitic bipolar transistor to operate is an effective way to improve avalanche capability. We have investigated the relationship between the P-base contact resistance, which is one of the factors that cause the parasitic bipolar transistor to operate, and avalanche capability, and have proposed process conditions to reduce the P-base contact resistance from the perspective of the mechanism of occurrence.

PO-019 Avalanche Capability Improvement by Ion Implantation-induced Defects Control for Trench Power MOSFET
Katsumi Rikimaru, TOSHIBA ELECTRONIC DEVICES & STORAGE
To improve the avalanche capability of trench
power MOSFETs, the resistance of the base diffusion layer must be lowered. Generally, a P-type high concentration layer is formed at the bottom of the trench. To form this layer, it is necessary to perform high-dose, low-energy boron implantation and activate it by annealing. However, if the diffused boron reaches the MOSFET channel, the threshold voltage will increase. In addition, high-dose ion implantation may result in EOR defects. BF2 and B were used as ion species in the P-type layer. The B ion was used at half the BF2 dose to prevent defect formation. The electrical characteristics of the two samples were compared, and the threshold voltage, on- resistance, and avalanche capability were the same as those of the BF2-implanted sample. Keywords— Trench power MOSFETs, avalanche capability, diffusion layer resistance, threshold voltage, crystal defects, P+ concentration profile"

Session B-3

PO-046 Ar/N2 gas flow rate dependence on the ferroelectric HfN1.15 thin film formation by ECR-plasma sputtering
KANGBAI LI, Tokyo Institute of Technology

In this paper, the Ar/N2 gas flow rate dependence on the ferroelectric HfNx formed by ECR-plasma sputtering was investigated. The equivalent oxide thickness (EOT) of 2.74 nm was obtained with Ar/N2 gas flow rate of 8/7 sccm followed by the 400°C/5 min post metallization annealing (PMA) in N2. The EOT was increased to 4.26 nm with the deposition of the Ar/N2 gas flow rate of 14/16 sccm. Moreover, as the gas flow rate increases, the Dit (density of interface states) also increases significantly.

YE-024 Investigation on the Relationship between Etching Rate and Photoresist Surface Temperature during Reactive Atmospheric-pressure Thermal Plasma Jet Irradiation Kyohei Matsumoto, Hiroshima University

Atmospheric-pressure reactive thermal plasma jet (R-TPJ) with Ar and O2 gas mixture was applied to etching of photoresist (PR) on silicon wafer. An optical interference contactless thermometry (OICT) and optical emission spectroscopy were carried out to clarify the relationship between the etching rate, PR surface temperature, and amount of atomic oxygen radicals. The results show that rapid temperature changes in the millisecond and supply of radicals by R-TPJ irradiation are the reasons of the ultra-fast etching.

PO-029 First-Principles Analysis for Estimating the Gettering Effects of Vacancy–Oxygen Complexes (VOx) in Rapid Thermal Processing Wafers Hiroya Iwashiro, GlobalWafers Japan

Rapid thermal process (RTP) treatment of Czochralski-grown Si wafers results in the formation of bulk vacancy-oxygen complexes (VOx). VOx is estimated to act as a nucleus for bulk micro defects (BMDs). VOx may have a metal gettering effect similar to that of BMDs. Therefore, this study investigates the potential for VOx to exhibit a gettering effect on significant metal impurities (Fe, Ni, and Cu) in the semiconductor manufacturing process, particularly in RTP wafers. The binding energy (Eb) was determined using first-principles calculation. The calculated Eb values for metastable VO4 and metals are 0.91, 0.84, and 0.98 eV for Fe, Ni, and Cu, respectively, all exceeding the Eb of Fe-B (0.65 eV). These results suggest that RTP wafers without BMD precipitation are likely to demonstrate a metal gettering effect.

Session B-4

PC-015 Virtual Metrology using Transfer Learning with Domain Knowledge
Masaaki Takada, Toshiba

Virtual Metrology (VM) is essential in semiconductor manufacturing for predicting wafer properties using sensor data. However, building accurate VM is challenging due to issues like high dimensionality and nonstationarity. Traditional methods such as Lasso perform feature selection and parameter estimation simultaneously; however they may conflict with domain knowledge. We introduce Weighted Transfer Lasso, a novel method that incorporates domain knowledge into the regression model. Experiments using reactive ion etching data demonstrate improved accuracy and consistency compared to traditional methods, highlighting its potential for reliable VM updates.

PC-009 Quick update of Virtual Metrology using Weighted Transfer Lasso
Kazuya Kikuchi, TOSHIBA ELECTRONIC DEVICES & STORAGE

This paper reports on a new update method for Virtual Metrology (VM). VM is a widely used technique in equipment quality control (QC) of semiconductor manufacturing. When using VMs in a semiconductor factory, VM models must be updated. The traditional approach is to collect a large amount of data over a long period to update the VM. We aim to update VM quickly, achieving high accuracy in a short period. To achieve this aim, we developed a new method called “Weighted Transfer Lasso”. In this paper, we report that it achieves high accuracy with quick update VM using Weighted Transfer Lasso. Weighted Transfer Lasso showed a higher correlation coefficient and reasonable variable selection. Therefore, when we launch the new 300mm equipment, we can achieve quick update of VM using Weighted Transfer Lasso.

Session B-5

PC-043 Fast Temperature Control in Semiconductor Vertical Furnace with Time-Optimal Control and Iterative Experiments Christian Milleneuve Budiono, The University of Tokyo

The semiconductor manufacturing industry continues to develop to meet the demand of semiconductor devices. Among various processes, the oxidation and layer deposition by semiconductor vertical furnace is known to be economic, yet due to its large size, has a relatively long process time. To raise its productivity rate, faster and high-precision temperature control are needed simultaneously. However, the presence of nonlinearity from the radiation heat transfer in the furnace caused the coexistence of fast and high-precision control by model-based approach to be more challenging. Therefore, the aim of this paper is to achieve faster temperature control in semiconductor vertical furnace while maintaining its precision by introducing a data-based approach in the time-optimal control framework. Experiments with full-scale semiconductor vertical furnace verified that the proposed method was able to raise the temperature accurately from 300 to 400°C in less than 10 minutes.

PC-030 Case Study on Modeling of Multiple Process Using Intermediate Variables for Digital Twin Modeling of a Semiconductor Manufacturing Ryosuke Okachi, Toyota Central R&D Labs., Inc.

digital twin models for multiple processes presents challenges owing to the dependence of subsequent processes on the previous results. In this study, we examined the issue of reduced model reusability caused by the dependency of process models on current process configurations. Using a case study involving the post-annealing and etching of an oxide film formed by atomic layer deposition, we developed a model that divided processes based on intermediate variables extracted through physical analysis. The results demonstrated that these intermediate variables sufficiently represented the impact of previous processes, with a high coefficient of determination indicating model effectiveness. Our analysis of the class structure emphasized the importance of confining variables within device classes for effective process abstraction. Applying this model design approach enhances process model abstraction and supports the model's suitability for representing the entire process.

PC-037 Improvement of Process Conditions using Hierarchical Optimization
Tatsuya Watanabe, Sony Semiconductor Manufacturing

This paper presents an application of hierarchical optimization to semiconductor manufacturing processes, focusing on thin film deposition in vertical furnaces. The applied method utilizes a two-layer hierarchical structure: the first layer determines optimal temperature conditions to improve wafer-to-wafer uniformity, while the second layer optimizes deposition time to achieve the target film thickness under the optimized temperature conditions. Experimental results demonstrate that, compared to the current method, this applied method improved wafer-to-wafer uniformity and reduced the number of iterations required to determine optimal conditions. This research advances semiconductor production by improving product quality and manufacturing efficiency, offering an effective approach to optimize complex processes.

Session B-6

ID-035 Classifiers and Clustering Based Approach for Imbalanced Wafer Map Data
Kenji Kanda, Mie University

In semiconductor manufacturing, wafer maps show defect distributions on wafers and help identify potential root causes. Effective identification relies on accurately grouping similar defect patterns. However, traditional supervised learning is costly, primarily due to the difficulty of collecting sufficient data for each defect pattern. Clustering methods address this, although they often fail to cluster infrequent defect patterns, risking undetected defects. We propose a hybrid method combining classification and clustering. Binary classifiers first detect frequent defect patterns, with clustering applied to the remaining data. Results show 48.5% average precision for infrequent defect patterns, representing a 43.2% improvement over conventional clustering alone.

ID-036 Unsupervised and Spectral Feature-based Sensor Relation Identification for Advanced Equipment Anomaly Detection Chieh-Yu Chen, National Taiwan University

Modern semiconductor fabrication relies on well-maintained and highly available equipment to ensure yield and productivity. Prompt anomaly detection (AD) using equipment sensory data (ESD) is critical for proactive maintenance. While exploiting sensor relations often improves AD accuracy and reduces delays, manual analysis is time-consuming and requires expert knowledge. In this paper, we propose a novel unsupervised test scheme, Spectral Analysis-based Log-log Slope Similarity (SALSS). It has two innovations: (i) the use, as spectral features, of regression slope and its standard error in the log-log plot to capture decaying speeds and fluctuation sizes of spectra in the learned normal ESD, and (ii) the use of t-test on the slope and F-test on the standard error to test similarity of two spectral features. A case study by using an HDP-CVD tool dataset shows that SALSS has 45.4% higher F1-score than the benchmark method for identifying relations, enhancing overall performance in AD.

ID-025 Generalized vs. Individualized Kaplan-Meier Time-to-Failure Predictive Models for Preventative Maintenance in Semiconductor Manufacturing Tori Wright, University of Central Florida

Accurate Remaining Useful Life (RUL) prediction is essential for effective predictive maintenance (PdM) in semiconductor manufacturing, reducing unplanned downtime and improving production efficiency. Survival analysis techniques are applied to model right-censored observations to accurately represent all tools in the plant, including those with incomplete failure data. In this paper, we develop individualized and generalized models to predict RUL for each tool in the plant. Generalized models represent the behavior of all tools, offering an efficient approach that can be applied even to tools with insufficient failure data. For tools with distinct failure patterns, individual models deliver more precise RUL estimates, enhancing the predictive accuracy and reliability of maintenance strategies.

Poster Session

PO-008 Optimization of post-deposition annealing conditions for p-type SnO fabrication by low-concentration hydrogen sputtering using SnO2 sputtering target Tsubasa Kobayashi, Kogakuin University

We fabricated SnO films from SnO2 target using a combined process of reductive sputtering and annealing at 800 °C. However, annealing for 30 min resulted in rough surface and precipitation of Sn due to disproportionation reaction. Here, we investigate the annealing conditions to obtain a smooth and uniform SnO film.

PO-011 Enhancing Process Engineering Decision-Making with Model Visualization Techniques
Hironori Chatani, ULVAC, Inc.

This paper examines the effectiveness of an interactive GUI for recipe adjustment in the PE-CVD process. By visualizing the relationship between film characteristics and parameters, we demonstrate that engineers can efficiently adjust recipes using their domain knowledge, even without expertise in data science. The experiment involved 41 batches of film deposition, and the GUI enabled the quantification of the impact of parameter variations on film properties. This approach is expected to enhance the efficiency and accuracy of process engineering.

ES-012 A New Operational Method for Green Transformation in Semiconductor Manufacturing
Toshiya Soyama, ULVAC, Inc.

This paper proposes a new operational concept for manufacturing processes to promote Green Transformation (GX) in semiconductor production. The proposed concept explores methods to achieve optimal production while maintaining product quality under power consumption constraints. This approach has the potential to optimize production while considering environmental measures, thereby creating economic value. We look forward to deepening discussions on industry challenges through the Interactive Poster Session.

PO-031 Fabrication of SnSO4 transparent thin-films using simultaneous oxidation and sulfurization annealing
Kento Moriya, Kogakuin University

$SnSO_4$ has a layered structure and is a promising candidate as a p-type transparent semiconductor with a band gap of 3.9 eV and hole effective mass of 0.88, theoretically. However, there has been no report on experimental fabrication of the semiconductor thin films. Here, we attempt trying fabrication of $SnSO_4$ thin films and investigating their electrical properties to clarify the possibility of SnSO4 thin films as p-type transparent semiconductors.

PO-038 UV exposure in an oxygen atmosphere at room temperature as a new method for improvement of amorphous oxide TFT characteristics Shinri Yamadera, Kogakuin University

Amorphous oxide semiconductors have attracted attention because of their low-temperature processability and high field-effect mobility. However, hysteresis remains in most case when the TFT channel is deposited at room temperature, thus heat treatments are generally required for the device fabrication. Here, we introduce room-temperature UV treatments being one possibility without heat treatment.

PO-040 Strong amorphization in In2O3-based flexible transparent conductive films by hydrogen incorporation and higher sputtering pressure Kanta Kibishi, Kogakuin University Flexible and transparent conductive films that can be processed at room temperature are strongly required. We have obtained the In2O3-based transparent thin-films with both conductivity and flexibility for next-generation electronic devices by changing hydrogen partial pressure during sputtering deposition, however, resistance degradation during bending test occurred. Here, we discuss the relationship between the resistance changes and sputtering conditions in Ar/H2 atmosphere.

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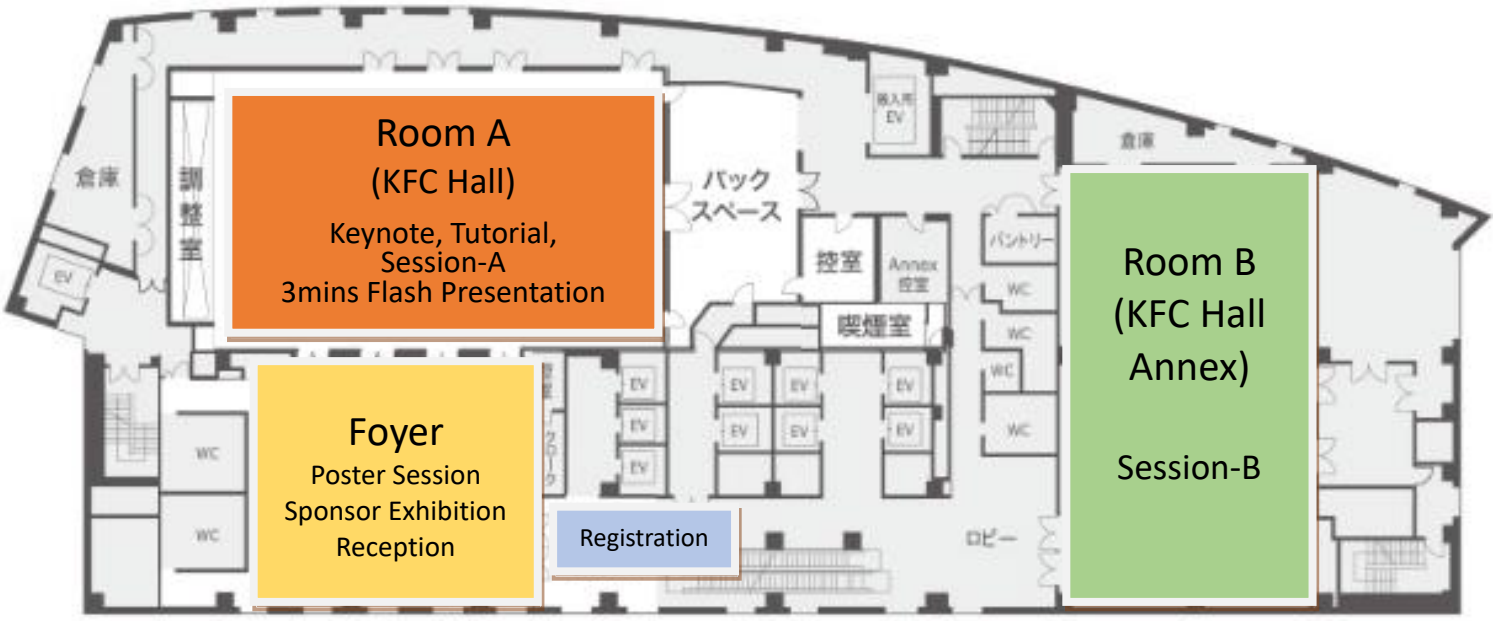

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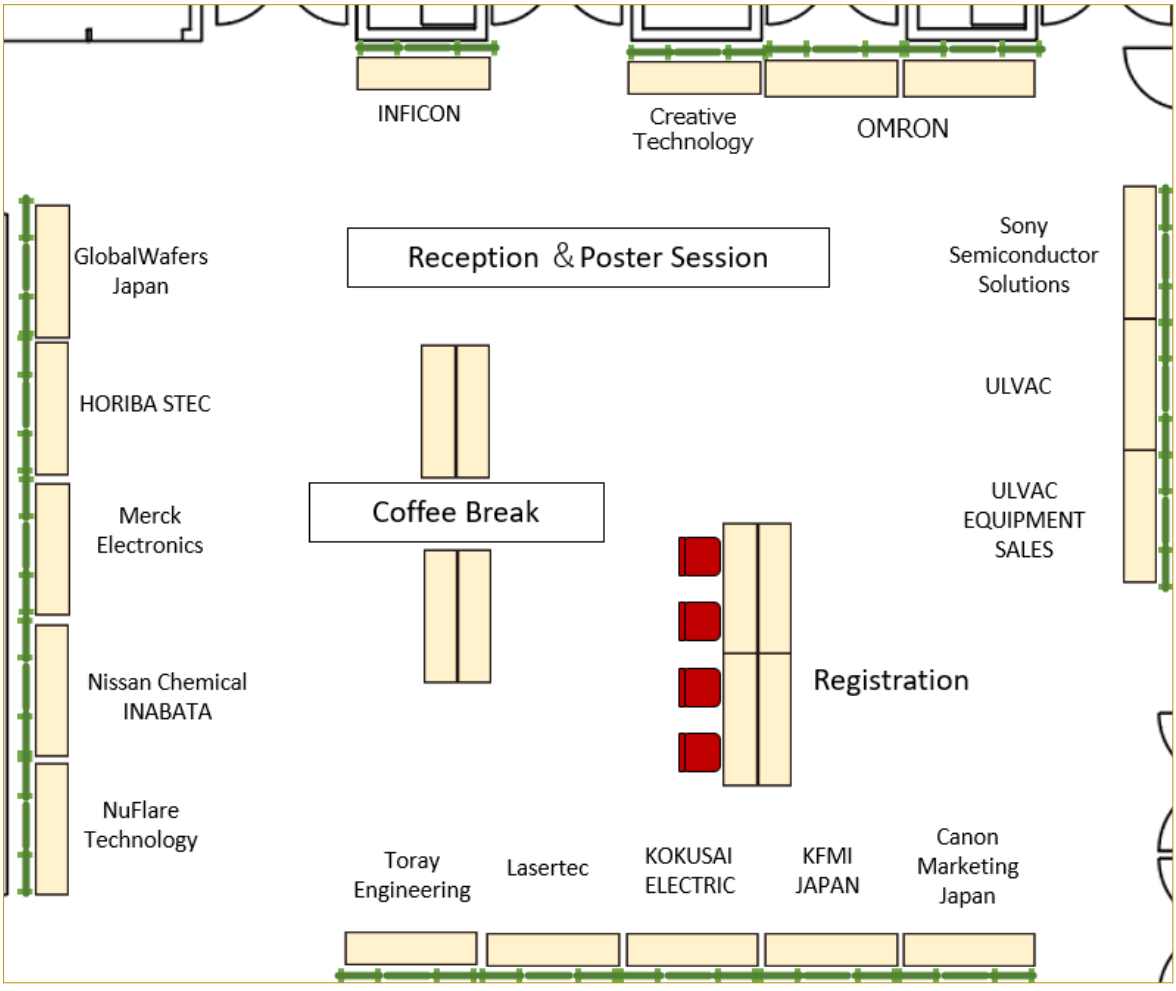

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Contact:

ISSM Office

Semiconductor Portal, Inc.

issm_2024@semiconportal.com