A Multi-step Wafer-level Run-to-Run Controller with Sampled Measurements for Furnace Deposition and CMP Process Flows - Joerg Reichelt[1]

Yulei Sun[1]/Tilo Bormann[2]/Andreas Gondorf[2]
Joerg.Reichelt@rudolphtech.com - Yulei.Sun@rudolphtech.com –
Tilo.Bormann@vishay.com - Andreas.Gondorf@vishay.com
[1]Rudolph Technologies, Inc., [2]Vishay Intertechnology, Inc.
1100 West Campbell Road, Richardson, TX 75080
Phone: +1 - (469) 624-4683 Fax: +1- (469) 624-4634

Traditionally, Run-to-Run (R2R) controllers for semiconductor manufacturing processes are mostly process-centric, meaning the R2R controllers are typically designed to solve the local control problems without aiming at the bigger picture of a series of steps. For example, considering a furnace deposition and CMP process flow as illustrated in Fig. 1, the majority of the post-CMP wafer-to-wafer thickness variation is coming from the drift in the post-deposition/pre-CMP thickness of wafers across the furnace tube (Fig. 2). A process-centric design philosophy will typically necessitate a multi-input-multi-output (MIMO) furnace controller to minimize the wafer-to-wafer thickness variation locally before it propagates to the downstream CMP process. An additional CMP control strategy would then need to be designed to compensate for the post-CMP wafer thickness variation introduced by the CMP tool drift. This traditional approach, however, can be complicated and difficult to implement and maintain, due to the MIMO nature of the furnace controller. Sometimes, it may require solving an optimization problem. Moreover, because of the batch processing of multiple lots at the same time in the furnace tube, it can be difficult to sufficiently compensate for process variations down to the lot and wafer level with limited process settings (e.g., deposition time, zone temperatures, etc.). Motivated by these considerations, a multiple-step control solution is developed in this work for a class of furnace deposition and CMP process flows. This approach aims to solve the control problems of both steps as a whole, and a wafer-level CMP controller with sampled pre- and post-CMP thickness measurements has been implemented with ProcessWORKS®, Rudolph Technologies' R2R framework.

With the bigger picture of the whole deposition-CMP process flow in mind, however, the compensation of the wafer-to-wafer thickness variation can also be performed at the CMP step, since the post-CMP thickness and uniformity are what really matter to the following lithography steps. To this end, a wafer-level CMP controller can be designed to calculate the polish time for each wafer in a lot, based on the pre-CMP thickness measurements of the current run and the post-CMP thickness measurements of previous runs. Typically, a wafer-level CMP controller requires measuring the incoming thickness of all wafers in a lot before the CMP step, which leads to an increase in the metrology cost and overall cycle time. When this CMP controller was developed in Vishay, it was observed that the pre-CMP thickness measurements can be approximated by a piecewise linear function (Fig. 3), and Vishay engineers performed full-lot measurements to confirm that a linear interpolation will sufficiently fit the real measurement values. As a result, the wafer-level control was still achieved for Vishay without measuring the full lot, by employing the knowledge of the upstream furnace deposition process and interpolating the missing incoming thickness values based on available samples with the help of ProcessWORKS' powerful mathematical functions. After the CMP step, the final thickness measurement is fed back to the controller, which then automatically updates the estimated removal rate to reflect the current machine and process state.

The integration of Vishay factory systems with ProcessWORKS was completed within three weeks, which allowed the CMP controller to be deployed within five weeks after the initial requirement gathering meeting. Since the deployment of this wafer-level CMP controller in production, the Cpk of the CMP process was increased by 72% with zero spec limit violation (Fig. 4). The post-CMP wafer-to-wafer thickness variation was also reduced by 70%. While the CMP tool drift and incoming wafer thickness variation had been successfully compensated for by the R2R controller, it was later discovered that the post-CMP thickness is also dependent on which furnace was used to process the wafer at the deposition step. To overcome the disturbance introduced by the furnaces, the R2R controller has been modified to include a correction factor of different values for different furnaces when calculating the polish times. This enhancement has improved Cpk by another 39%.

Figure 1: Process flow of furnace deposition and CMP

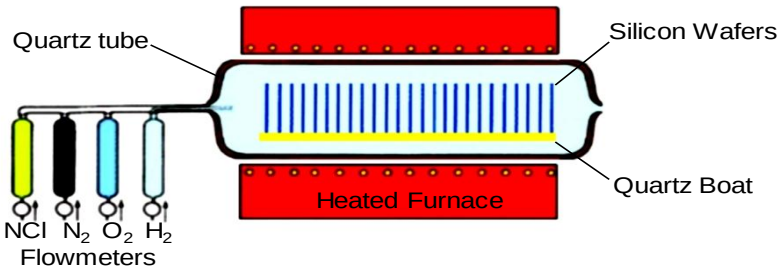

Figure 2: Batch processing of wafers in a furnace

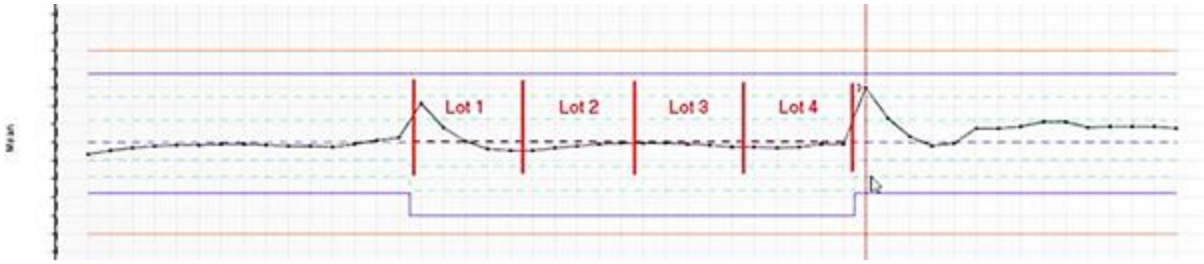

Figure 3: SPC chart of pre-CMP thickness metrology values after furnace deposition step

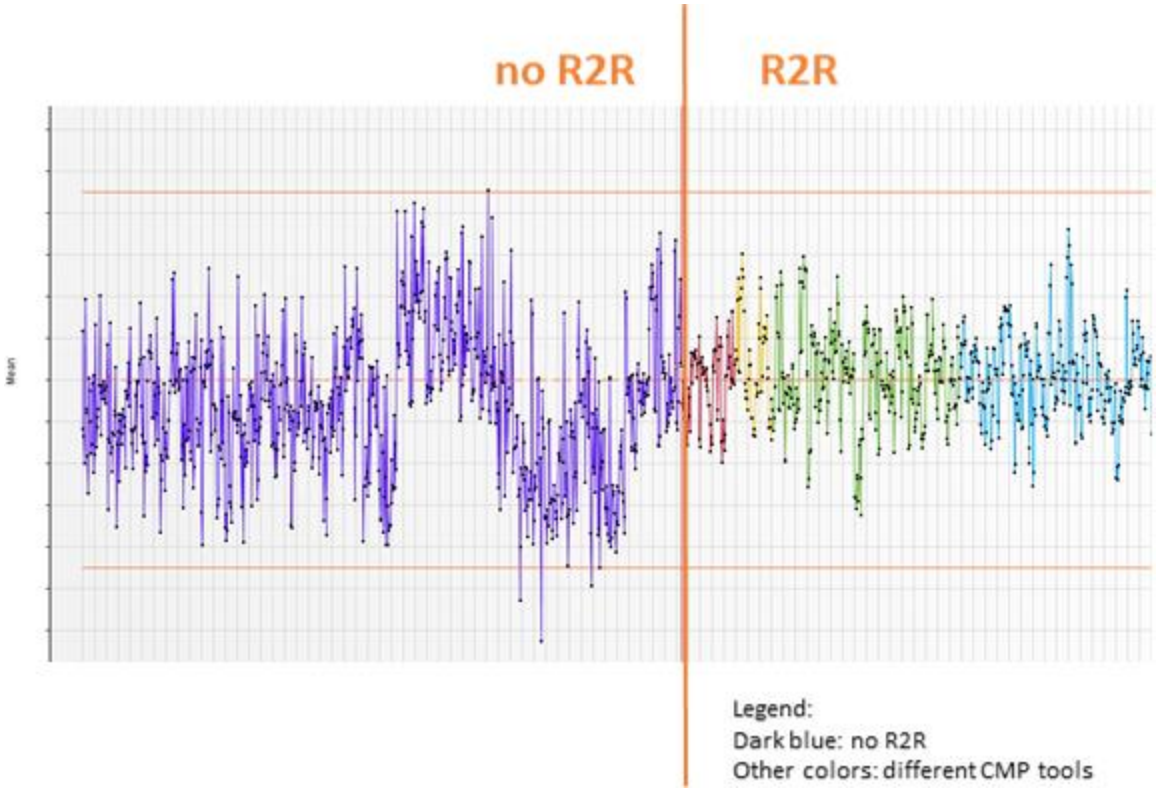

Figure 4: Comparison of SPC charts before and after R2R was implemented for CMP