

Semiconductor Tool Monitoring by integrating defect signatures and in-line WIP

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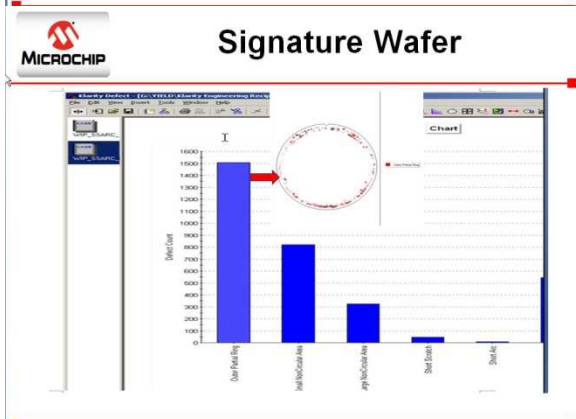
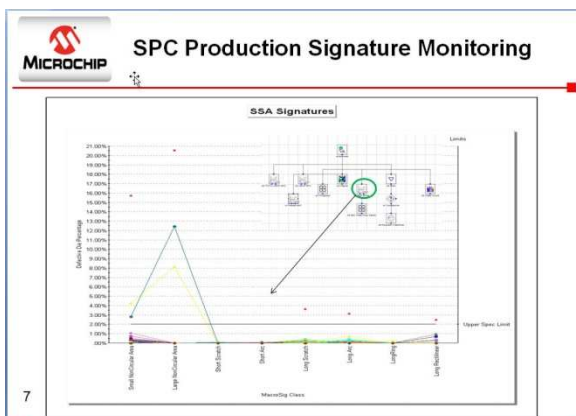
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Abstract

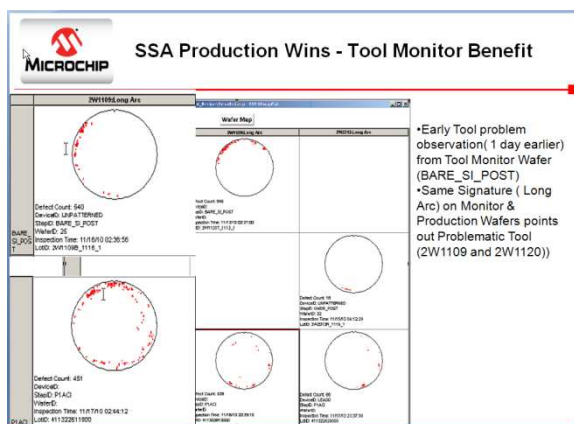
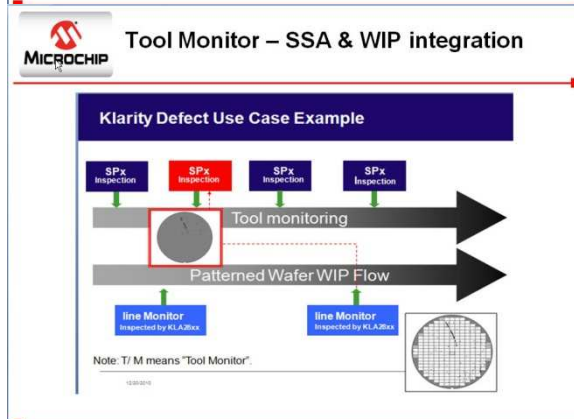
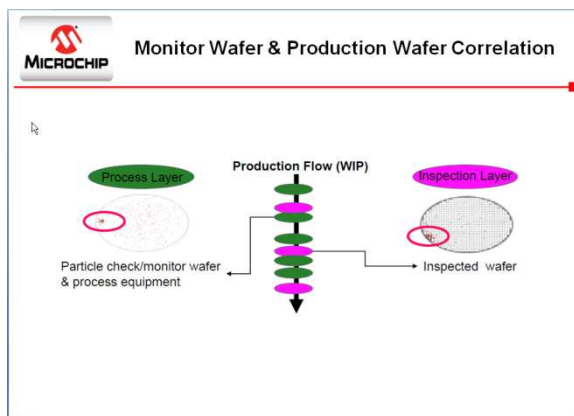
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Many semiconductor Fabs are using monitor wafers to qualify chip manufacturing tools. Due to high tool utilizations, mismatched qualification recipes and complexity factors it is difficult to accurately monitor the health of the process tool. In a high volume manufacturing environment it is imperative that reaction to monitor wafer failures is addressed expediently so as to contain the process equipment, impacted material and minimize the risk to product yield. Most fabrication facilities use a measure of total defectively as an indicator to the health of the process. When there is an excursion or failure identifying the process chambers/load position that is responsible for the failure is often a tedious process that requires many man hours. Klarity Spatial Signature Analysis (SSA) allows a real-time monitor of defect signatures on product and monitor wafers which is correlated to either the process tool, handling or material related causes. Integration of SSA with Wafer In Process (WIP) provides automation of defect data with visibility into problematic process tools and chamber-to-chamber or tool-to-tool variation on defectively levels.

This paper provides a user methodology on the use of SSA and WIP in a high volume manufacturing environment that clearly demonstrates the benefits of Klarity SSA and WIP modules to improve reaction time, minimize risk to impacted product and quick identification of "run-away" tools.



Wafer Signature Monitoring



Wafer Process Tool Monitoring