2013 IEEE International
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June 13-15, 2013 Kyoto Research Park, Kyoto, Japan

TECHNICAL SESSIONS

June 15, 2013

12:45-15:05

Session 12: 3D Integration II
Session Co-chairs:
Tetsu Tanaka, Tohoku University
Kenichi Takeda, Hitachi

12:45-13:15

12-1 ***INVITED - Development of 3D-stacked Reconfigurable Spin Logic Chip using Via-last Backside-via 3D Integration Technology***

Tetsu Tanaka
Tohoku University, Japan

<Abstract>
The paper will cover process technology of ultrafast on-chip SPRAM and 3D-stacked structure as well as performance of reconfigurable logic chip using the 3D LSI which could overcome the drawbacks of conventional reconfigurable LSIs. The proposed 3D-LSI consists of several reconfigurable spin logic layers with on-chip SPRAMs and processor array layer. These layers are stacked and connected with high density Through-Si Vias (TSVs). This combination could provide both high-speed circuit configuration and parallel reconfiguration. The paper will highlight key process technologies including back-side TSV formation to SPRAM chip and low temperature microbump connection.

13:15-13:40

12-2 ***Novel Through-Silicon via Technologies for 3D System Integration***

Paragkumar Thadesar, Ashish Dembla, Devin Brown, Muhannad Bakir
Georgia Institute of Technology, United States

<Abstract>
To circumvent the performance and energy bottlenecks due to interconnects, novel interconnect solutions are needed both at the package and die levels. This paper reports (1) novel photodefined polymer-embedded vias within silicon interposers for improved through-silicon via insertion loss, and (2) ultrahigh density low-capacitance nanoscale TSVs with 100 nm diameter and 20:1 aspect ratio for fine grain 3D IC implementation.

13:40-14:10

12-3 ***INVITED - Interconnection Requirements and Multi-Die Integration for FPGAs***

Arif Rahman, J. Schulz, R. Grenier, K. Chanda, M.J. Lee, D. Ratakonda, H. Shi, Z. Li, K. Chandrasekar, J. Xie, and D. Ibbotson
Altera, United States

<Abstract>
Die stacking technology with high-density interconnect is enabling new product architectures and capabilities. Silicon interposer based stacking with through silicon via (TSV) has gained traction for high performance applications. Some of the challenges in manufacturing technology, supply-chain strategy, design tools and infrastructure are being addressed to enable broader technology adoption. This paper provides an overview of Field Programmable Gate Array (FPGA) application trends which are driving the need for advanced die-stacking technologies. We present design and manufacturing considerations for stacking technologies and highlight lessons learned from a recent technology demonstration vehicle.

14:10-14:35

12-4 ***System-Level Analysis for 3D Interconnection Networks***

Chenyun Pan, Azad Naeemi
Georgia Institute of Technology, United States

<Abstract>

This paper provides a fast and efficient approach to analyze and compare systems implemented with through-silicon via (TSV) and monolithic inter-tier via (MIV) 3D integration technologies based on compact models for cycle-per-instruction, memory throughput, and multi-level interconnect networks. Additionally, the impact of via diameter and capacitance on the overall system throughput has been quantified. It is demonstrated that for the same die area and thermal constraint, an MIV-based processor offers over 25% improvement in computational throughput as compared with its 2D counterpart.

14:35-15:05

12-5 ***INVITED - 3D Integration challenges today: From technological toolbox to industrial prototypes***

Thierry Mourier
Leti, France

<Abstract>

3D Integration challenges today: From technological toolbox to industrial prototypes 3D integration has been widely described and studied during past years and technological modules and processes were developed for a wide range of applications requested from industry. Today, the integration maturity has reached a manufacturing worthy state and several demonstrators were realized for various products such as advanced interposers, Memory on Logic for mobile applications as well as small volume specific requests for integrated sensors. The talk (or paper) will present the challenges assessed by the toolbox concept in terms of design, modelization and technological modules, discuss on the definition and ramp up of a complete pilot line dedicated to prototyping of 3D demonstrators for various applications from industrial partners and designed to be compatible with processing of wafers coming from and going back to manufacturing facilities. Then, results of fully functional demonstrators obtained through 3D integration and issued from this 300 mm pilot line will be presented and detailed.

15:05-15:20 **Break**