TECHNICAL SESSIONS

June 15, 2013

10:40-11:30

Session 11: Process Integration III
Session Co-chairs:
Susumu Matsumoto, Panasonic
Nae-In Lee, Samsung Electronics

10:40-11:05

11-1 ***CVD-Co/Cu(Mn) Integration and Reliability for 10 nm Node***

Takeshi Nogami{2}, Ming He{1}, Xunyuan Zhang{1}, Kunaljeet Tanwar{1}, Raghuveer Patlolla{1}, James Kelly{2}, David Rath{2}, Mahadevaiyer Krishnan{2}, Xuan Lin{1}, Oscar Straten{2}, Hosadurga Shobha{2}, Juntao Li{2}, A. Madan{2}, P. Flaitz{2}, C. Parks{2}, Chao-Kun Hu{2}, C. Penny{2}, A. Simon{2}, T. Bolom{1}, J. Maniscalco{2}, D. Canaperi{2}, Terry Spooner{2}, D. Edelstein{2}
{1}Global Foundries Inc., United States; {2}IBM Corp., United States

<Abstract>
The mechanism of Co liner enhancement of Cu gap-fill was identified to be a wetting improvement of the PVD Cu seed, rather than a local nucleation enhancement for Cu plating. Co gdivot h (top-corner slit void defect) formation can be suppressed by a new wet chemistry, in turn eliminating divot-induced EM degradation. Cu-alloy seed proportional resistivity impact decreased relatively compared to scattering at scaled dimensions. Oxygen at the TaN/CVD-Co interface consumes Mn atoms to diminish Mn segregation at the Cu/cap interface and EM benefits. O-free CVD-Co may solve this problem enabling CVD-Co/Cu-alloy seed integration in advanced nodes.

11:05-11:30

11-2 ***Demonstration of a 12 nm-Half-Pitch Copper Ultralow-K Interconnect Process***

Jasmeet Chawla, Ramanan Chebiam, Rohan Akolkar, Gary Allen, Colin Carver, James Clarke, Florian Gstrein, Michael Harmes, Tejaswi Indukuri, Christopher Jezewski, B. Krist, H. Lang, A. Myers, Richard Schenker, K. J. Singh, R. Turkot, Hui Jae Yoo
Intel, United States

<Abstract>
A process to achieve 12 nm half-pitch interconnect structures in ultralow-k interlayer dielectric (ILD) is realized by pitch division using standard 193 nm lithography. An optimized pattern transfer that minimizes unwanted distortion of ILD features is followed by copper fill. Cross section images and electrical measurements that validate functionality of the drawn structures are presented.

11:30-12:45 **Lunch**