TECHNICAL SESSIONS

June 15, 2013

09:00-10:20

Session 10: Process Integration II

Session Co-chairs:
Nae-In Lee, Samsung Electronics
Susumu Matsumoto, Panasonic

09:00-09:30

10-1 ***INVITED - 48nm pitch Cu Dual-Damascene Interconnects using Self Aligned Double Patterning Scheme***

Shyng-Tsong Chen{2}, Tae-Soo Kim{3}, Seo-woo Nam{1}, Neal Lafferty{2}, Chiew-Seng Koay{2}, Nicole Saulnier{2}, Wenhui Wang{1}, Yongan Xu{2}, Benjamin Duclaux{4}, Yann Mignot{4}, Marcy Beard{2}, Yunpeng Yin{2}, Hosadurga Shobha{2}, Oscar Van der Straten{2}, Ming He{1}, James Kelly{2}, Matthew Colburn{2}, Terry Spooner{2}
{1}Global Foundries, United States; {2}IBM, United States; {3}Samsung Electronics, United States; {4}STMicroelectronics, United States

<Abstract>
For sub-64nm pitch interconnects build, it is beneficial to use Self Aligned Double Patterning (SADP) scheme for line level patterning. Usually a 2X pitch pattern was printed first, followed by a Sidewall Image Transfer (SIT) technique to create the 1X pitch pattern. A block lithography process is then used to trim this pattern to form the actual designed pattern. In this paper, 48nm and 45nm pitch SADP build will be used as examples to demonstrate the SADP patterning scheme. General discussions about this patterning scheme will be provided including: 1) the process flow of this technique, 2) benefits of the technique vs. pitch split approach, 3) the design impact and limitation, and 4) the extendability to smaller line pitch build.

09:30-09:55

10-2 ***UV Cure Impact on Robust Low-K with Sub-nm Pores and High Carbon Content for High Performance Cu/Low-K BEOL Modules***

Naoya Inoue{3}, Fuminori Ito{3}, Hosadurga Shobha{2}, Stephen Gates{2}, Todd Ryan{1}, Kumar Virwani{2}, Nancy Klymko{2}, A. Madan{2}, L. Tai{2}, E. Adams{2}, S. Cohen{2}, Eric Liniger{2}, Chao-Kun Hu{2}, Yann Mignot{4}, A. Grill{2}, Terry Spooner{2}
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<Abstract>
UV cure on robust low-k with sub-nm pore and high carbon content (R-ELK=Robust ELK) was studied to enhance the modulus of the film. UV cure helps to create Si-CH2-Si bridging bond, which plays a role to enhance the modulus. UV cure does not affect the advantage of low PID (plasma-induced damage) and it was confirmed by Cint (interconnect capacitance) measurement for 80 nm pitch interconnect. Besides, UV cured R-ELK demonstrated high TDDB and EM reliability, with lifetime similar to the mature ULK baseline. High TDDB reliability with further dimensional scaling was also confirmed for the test structure with 20 nm spacing.

09:55-10:20

10-3 ***New Fluorocarbon Free Chemistry Proposed As Solution to Limit Porous SiOCH Film Modification During Etching***

Nicolas Posseme{2}, Laurent Vallier{3}, Chia-Ling Kao{1}, Christophe Licitra{2}, Camille Petit-Etienne{3}, Cedric Mannequin{3}, Patrice Gonon{3}, Sergey Belostotskiy{1}, Jerehmia Pender{1}, Sebastien Barnola{2}, Olivier Joubert{3},

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<Abstract>
Today porous SiOCH combined with metallic hard masking strategy is an integration of choice for advanced BEOL interconnect technology node. However in this context the main integration issue is the dielectric film sensitivity to fluorocarbon (FC) etch chemistry. In this study, new FC free etching chemistry has been proposed as breakthrough solution. Based on pattern and blanket film analyses, the benefits of this new chemistry is presented and discussed with respect to conventional FC etching. Its compatibility with metallic hard mask integration and wet cleaning is also evaluated.

10:20-10:40 **Break**