TECHNICAL SESSIONS

June 14, 2013

15:00-16:20

Session 8: 3D Integration I
Session Co-chairs:
Azad Naeemi, Georgia Institute of Technology
Kenichi Takeda, Hitachi

15:00-15:30

8-1 ***INVITED - Reliability Challenges of Through-Silicon-Via (TSV) Stacked Memory Chips for 3-D Integration: from Transistors to Packages***

Ho-Young Son, Woong-Sun Lee, Seung-Kwon Noh, Min-Suk Suh, Jae-Sung Oh, Nam-Seog Kim
SK Hynix, Korea, South

<*Abstract*>
Recently, three-dimensional stacked chip package using through-silicon vias (TSVs) is a major paradigm which leads the transition of semiconductor technology from 2-D to 3-D IC in the electronic industry. However, lots of reliability concerns lie in the developing stage and we should clear away doubtful suspicion prior to mass production of 3-D stacked chip package. In this paper, an overview of reliability issues of 3-D TSV integration is introduced dividing into three categories: zero-level reliability of FEOL (front-end of the-line) such as transistors and capacitors, 1st level of BEOL (back-end of the-line) metallization and TSV interconnections, and 2nd level of micro-bumps of stacked chip interfaces. This paper describes the essential scope of the reliability challenges in 3-D IC packaging technology by dealing with reliability issues from transistor-level of the memory device to package micro-bump level of chip-to-chip interconnections.

15:30-15:55

8-2 ***Impact of Material and Microstructure on Thermal Stresses and Reliability of Through-Silicon via (TSV) Structures***

Tengfei Jiang{3}, Suk-Kyu Ryu{1}, Jay Im{3}, Ho-Young Son{2}, Nam-Seog Kim{2}, Rui Huang{3}, Paul Ho{3}
{1}Applied Materials Inc, United States; {2}SK Hynix Inc, Korea, South; {3}University of Texas at Austin, United States

<*Abstract*>
Thermal stresses and microstructures of two TSV structures with different fabrication conditions have been investigated using the precision wafer curvature and synchrotron x-ray microdiffraction methods, providing the first direct observation of local plasticity in the TSVs. Microstructure studies by EBSD, chemistry analysis by TOF-SIMS and nanoindentation measurements were also conducted. Results from this study show that the electroplating chemistry directly affects the Cu microstructure, which in turn controls stress relaxation and build-up of the residual stress during thermal cycling. The implications on via extrusion and device keep-out zone (KOZ) are discussed.

15:55-16:20

8-3 ***Investigations on Partially Filled HAR TSVs for MEMS Applications***

Lutz Hofmann, Ina Schubert, Knut Gottfried, Stefan E. Schulz, Thomas Gessner
Fraunhofer ENAS, Germany

<*Abstract*>
This paper presents technological aspects for the vertical integration of MEMS Devices using HAR-TSV. For considerations of stress reduction the TSVs were only partially filled with copper. A comparison was made to ring shaped TSVs (i.e.

copper ring with silicon core). Two approaches regarding the way of TSV implementation (before and after wafer bonding/ thinning, resp.) are discussed, concerning process ability and yield aspects. Electrical measurement yield 11 mΩ; for a single TSV and 76 mΩ; for a 4-point TSV-chain (incl. RDL).

16:20-16:40 **Break**