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TECHNICAL SESSION

June 14, 2013

13:30-15:00 Session 7: Poster Session

7-1 ***Early Screening Method of Chip-Package Interaction for Multi-Layer Cu/Low-K Structure Using High Load Indentation Test***

Tatsuya Usami, Tomoyuki Nakamura, Iwao Yashima
Renesas Electronics Corporation, Japan

<Abstract>
We have developed High Load Indentation test as a novel early screening method of Chip-Package Interaction for multi-layer Cu/Low-k interconnects structure with bumps. In this study, by using HiLI test, we evaluated a lower fracture toughness SiCOH, a thicker under bump metallization and a plasma-damaged polyimide around these bumps, whose white bump failures relatively tend to occur compared to the standard structure. We found that both these in-situ load profiles and observations after the test corresponded with these white bump failures. In addition, we compared between a polished bump structure and an un-polished bump one by the test.

7-2 ***Early Failure of Short-Lead Metal Line and its Em Characterization with Wheatstone Bridge Test Structure in Advanced Cu/ULK BEOL Process***

Tae-Young Jeong, Sari Windu, Dong-Cheon Baek, Jinseok Kim, Kyuho Tak, Miji Lee, Hyunjun Choi, Sangwoo Pae, Jongwoo Park
Samsung Electronics, Korea, South

<Abstract>
Early failure of the short-lead metal EM (Electromigration) is investigated. Applying Wheatstone bridge (WSB) test structure and 3-parameter lognormal distribution enables to reduce sample size and time-to-fail (TTF) variation governed by early fails causing a poor standard deviation, EM lifetime is accurately predicted and improved by ~280x. In particular, EM TTF at lower percentiles can be well represented by 3-parameter lognormal. With respect to physical aspects of void, EM behaviors of the short-lead and long-lead metal line are addressed based on experimental results compared with Monte-Carlo simulations to support the Blech's back-stress effects.

7-3 ***Redundancy Method to Assess Electromigration Lifetime in Power Grid Design***

Boukary Ouattara{3}, Lise Doyen{2}, David Ney{2}, Habib Mehrez{1}, Pirouz Bazargan-Sabet{1}, Franck Lionel Bana{2}
{1}Laboratory of Computer Sciences, Paris 6 (LIP6), France; {2}STMicroelectronics, France; {3}STMicroelectronics/Laboratory of Computer Sciences, Paris 6 (LIP6), France

<Abstract>
The tendency of semiconductor market to increase component density in small chip leads to reliability issues such as Electromigration (EM). This phenomenon becomes critical in deep submicron design technology. In this paper we assess chip power grid lifetimes by taking into account redundant paths contribution in case of EM degradation. The application of this method for wire lifetime validation of a 32nm microprocessor has reduced significantly wires susceptible to EM given by simulation tools.

7-4 ***Compact Modeling and Optimization of Fine-Pitch Interconnects for Silicon Interposers***

Vachan Kumar, Li Zheng, Muhannad Bakir, Azad Naeemi
Georgia Institute of Technology, United States

<Abstract>

This paper presents the first optimization methodology for silicon interposer interconnect technology. The dimensions of these fine-pitch interconnects are roughly a few microns, because of which they can neither be treated as on-chip RC interconnects, nor as conventional off-chip interconnects. 3D extraction tools can provide an accurate estimate of the circuit parameters, but they prove to be very slow and tedious for design space exploration and optimization. Thus, the novel analytical models developed here for the frequency dependent resistance of fine-pitch interconnects are essential to efficiently optimize these interconnects. The error in the model is shown to be less than 15% for interconnect dimensions and frequency range of interest. The analytical models developed are then used to optimize the data-rate and cross-sectional dimensions to maximize the bandwidth-density and minimize the energyper-bit, simultaneously.

7-5 *Low Temperature Bonding of Sn/In-Cu Interconnects for Three-Dimensional Integration Applications*

Ruoh-Ning Tzeng{2}, Yan-Pin Huang{2}, Yu-San Chien{2}, Ching-Te Chuang{2}, Wei Hwang{2}, Jin-Chern Chiou{2}, Ming-Shaw Shy{1}, Kuan-Neng Chen{2}, Teu-Hua Lin{1}, Kou-Hua Chen{1}, Chi-Tsung Chiu{1}, Ho-Ming Tong{1}

{1}Advanced Semiconductor Engineering Group, Taiwan; {2}Department of Electronics Engineering, National Chiao Tung University, Taiwan

<Abstract>

A low temperature bonding technology of Sn/In composite solder bonded to Cu interconnect is proposed and investigated. The intermetallic compounds formed in the bonded interconnects can survive well in the following process. The Sn/In-Cu interconnects bonded at low temperature all exhibit excellent electrical performance and high resistance to multiple current stressing, showing a great potential in 3D applications.

7-6 *Thin Nickel Films Growth Using Plasma Enhanced Atomic Layer Deposition from η^3-2-methylallyl N,N'-diisopropylacetamidinate Nickel(II)*

Jiro Yokota{1}, Clement Lansalot{2}, Changhee Ko{1}

{1}Air Liquide Laboratories, Japan; {2}Air Liquide Laboratories Korea, Korea, South

<Abstract>

2-methylallyl-N,N'-diisopropylacetamidinate nickel(II) is a promising precursor for the deposition of pure nickel film to be later used in the silicidation process. High purity, high deposition rate, low resistivity of the film and good step coverage were successfully confirmed for the deposition of pure metal nickel films.

7-7 *Annealing Effect on the Structure Characteristics of Nano-Scale Damascene Copper Lines*

Tatyana Konkova{1}, Sergey Mironov{2}, Yiqing Ke{1}, Jin Onuki{1}

{1}Ibaraki University, Japan; {2}Tohoku University, Japan

<Abstract>

High-resolution electron backscatter diffraction (EBSD) technique was applied for systematic and detailed study of grain structure and texture changes in various microstructural regions of nano-scale damascene copper lines after annealing in a wide temperature range of 200-500C. To ensure reliability of the obtained results, large EBSD maps including several thousand grains were obtained in each case. Above 200 C, the grain structure was established to be surprisingly stable in both the overburden layer as well as within the lines. The grain growth in the lines was supposed to be suppressed by pinning effect of second-phase particles entrapped during electrodeposition process.

7-8 ***Endpoint Detection Using Optical Emission Spectroscopy in TSV Fabrication***

Ja Myung Gu{1}, Paragkumar Thadesar{1}, Ashish Dembla{1}, Sang Jeen Hong{2}, Muhannad Bakir{1}, Gary May{1}
{1}Georgia Institute of Technology, United States; {2}Myongji University, Korea, South

<Abstract>
A hybrid partial least squares-support vector machine (PLS-SVM) model of optical emission spectroscopy data is proposed and successfully demonstrated to predict the endpoint detection of through silicon vias (TSVs) etched using the Bosch process. Accurate results are shown for TSVs with diameters of 80 μm and 25 μm.

7-9 ***WITHDRAW***

7-10 ***Beam-Substrate Interaction During Tungsten Deposition by Helium Ion Microscope***

Kazuyuki Kohama, Tomohiko Iijima, Misa Hayashida, Shinichi Ogawa
National Institute of Advanced Industrial Science and Technology(AIST), Japan
(K.Kohama recently moved to JWRI, Osaka University、Japan)

<Abstract>
We deposited tungsten-based pillars on about 300 nm-thick carbon and silicon substrates by a helium ion microscope using W(CO)6 as a gaseous precursor. We then investigated beam-induced damage to the substrates correlated with both pillar growth rate and material type of substrates. Faster pillar growth reduced the substrate damage because the pillars shielded the substrates from the incident beam, resulting in a low-damage process. On the other hand, the Si substrate was significantly damaged by the incident beam compared with the carbon substrates. This is because stopping cross-section of 30-keV helium ion in silicon is about 1.5 times higher than that in carbon. The incident helium ions were considered to induce the substrate damage in the process of losing energy in the substrates.

7-11 ***Development and Evaluation of a-SiC:H Films Using a dimethylsilacyclopentane Precursor As a Low-K Cu Capping Layer***

Els Van Besien, Cong Wang, Patrick Verdonck, Arjun Singh, Yohan Barbarin, Jean-François de Marneffe, Kris Vanstreels, Hilde Tielens, Marc Schaekers, Mikhail R. Baklanov, Sven Van Elshocht
IMEC, Belgium

<Abstract>
Scaling of the Cu interconnect structures requires Cu capping layers with an increasingly lower dielectric constant that still have adequate Cu and moisture barrier properties. In this work, we study the plasma enhanced chemical vapour (PE-CVD) deposition of amorphous silicon carbide films using dimethyl silacyclopentane (DMSCP) as a precursor, resulting in the incorporation of Si-(CH2)n-Si bridges. The effect of process parameters on film characteristics like dielectric constant, mass density, and leakage behaviour is investigated, as well as their relation with the chemical bonding structure. Finally, Cu barrier properties and hermeticity are evaluated.

7-12 ***Stress Reduction Induced by Bosch Scallops on an Open TSV Technology***

Anderson Singulani, Hajdin Ceric, Erasmus Langer
Technical University of Vienna, Austria

<Abstract>
Through Silicon Via (TSV) is a lead topic in interconnects and 3D integration research, mainly due to numerous anticipated advantages. However, several

challenges must still be overcome if large scale production is to be achieved. In this work, we have studied effects of Bosch scallops concerning mechanical reliability for a specific TSV technology. We identified that the presence of scallops on the TSV wall modifies the stress distribution. The achieved results support experiments and give a better insight into the influence of scallops in an open TSV.

7-13 ***Fabrication and Electrical Characterization of 5x50um Through Silicon Vias for 3D Integration***

Bharat Bhushan, Minrui Yu, John Dukovic, Loke Yuen Wong, Aksel Kitowski, Mun Kyu Park, John Hua, Shwetha Bolagond, Anthony C-T Chan, Chin Hock Toh, Arvind Sundarrajan, Niranjan Kumar, Sesh Ramaswami
Applied Materials, United States

<Abstract>
We present fabrication, electrical characterization, and metrology analysis results of 5×50um TSVs for 3D integration. Specifically, electrical performance of blind TSVs is evaluated by capacitance-voltage (CV) and current-voltage (IV) measurements. Important electrical parameters such as oxide capacitance, minimum TSV capacitance, leakage current, and breakdown voltage are extracted and show good results. The capacitance values also closely match model predictions. The electrical testing data are further verified with a variety of materials analysis techniques.

7-14 ***Electrical Properties of Multilayer Graphene Interconnects Prepared by Chemical Vapor Deposition***

Masayuki Katagiri, Hisao Miyazaki, Yuichi Yamazaki, Li Zhang, Takashi Matsumoto, Makoto Wada, Akihiro Kajita, Tadashi Sakai
Low-power Electronics Association & Project (LEAP), Japan

<Abstract>
We fabricate multilayer graphene interconnects with 100-nm-class line widths. Multilayer graphene is grown on a Ni catalyst layer using remote plasma-enhanced chemical vapor deposition (CVD) at a low temperature of 600 °C and transferred onto a SiO_2/Si substrate after exfoliation from the Ni layer. The sheet resistance of the CVD graphene interconnects is as low as 500 Ω/sq. The temperature dependence of resistance reveals that the CVD graphene exhibits half-metallic transport properties.

7-15 ***Advanced Nanostructured Materials Applied in Nanoelectronics***

Hui Lin Chang, Waylon Mcguigan
National Chiao Tung Univ, Taiwan

<Abstract>
A systematic work of random oriented SiCN tubes, nanowire/conical rod and 2-D graphite/seaweed structures are covered and their corresponding properties have been reached in this study. The growth mechanism and electronic properties of nanostructured materials have been addressed. The development of nanostructured materials is crucial in enhancing emerging devices application.

7-16 ***Numerical Simulations of High Heat Dissipation Technology in LSI 3-D Packaging Using Carbon Nanotube Through Silicon via (CNT-TSV) and Thermal Interface Material (CNT-TIM)***

Teppei Kawanabe[1], Akio Kawabata[2], Tomo Murakami[2], Mizuhisa Nihei[2], Yuji Awano[1]
[1]Keio University, Japan; [2]National Institute of Advanced Industrial Science and Technology, Japan

<Abstract>

We report numerical simulations of heat dissipation properties of nano-carbon through silicon via (TSV), thermal interface material (TIM), and chip package towards a high power heat dissipation LSI 3-D packaging. By using vertically aligned multi-walled CNTs (MWNTs) as both TSV and TIM materials and graphite as chip package, a boundary temperature just under a heat source decreased 40.8K in total, comparing to that using conventional materials. This result suggests superior heat dissipation properties of nano-carbon 3-D packaging.

7-17 ***Development of Sputtering Technology of Ta_2O_5/TaO_x Stacked Film for ReRAM Mass-Production***

Natsuki Fukuda, Kazunori Fukuju, Yutaka Nishioka, Koukou Suu
ULVAC, Inc., Japan

<Abstract>

This paper deals with development of sputtering technology of Ta2O5/TaOx stacked film for ReRAM mass-production. Thickness of TaOx film deposited by sputtering process is possible to obtain with good uniformity. However, if a high deposition rate is required for mass production, it is very difficult to obtain good controllability and uniformity of TaOx film. These problems affect the switching characteristics of the ReRAM. In order to solve these problems, sputtering tool and process for ReRAM mass-production are developed. We report the result of TaOx film with good resistance uniformity and controllability and deposition stability without low deposition rate. Moreover, switching characteristics of Pt/Ta2O5/TaOx/Pt-ReRAM-cells are evaluated.