TECHNICAL SESSIONS

June 13, 2013

15:45-18:00

Session 4: Packaging
Session Co-chairs:
Takeshi Furusawa, Renesas Electronics
Tomoji Nakamura, Fujitsu Labs

15:45-16:15

4-1 ***INVITED - Experimental Analysis of Mechanical Stresses and Material Properties in Multi-Layer Interconnect Systems by fibDAC***

Dietmar Vogel, Ellen Auerswald, Bernd Michel, Sven Rzepka
Fraunhofer ENAS, Germany

<*Abstract*>
The paper presents a new stress measurement method on base of stress relief caused by local material removal with ion milling in FIB equipment. Stress relief deformations extracted from SEM micrographs by means of digital im-age correlation allow the determination of stresses, as well as to estimate Young's modulus on the position of ion milling. The paper gives an introduction into the method. The feasibility to extract local stresses in multilayer stacks, both in lateral direction and in depth, is discussed in more detail.

16:15-16:40

4-2 ***Modeling of Interconnect Stress Evolution During BEOL Process and Packaging***

Chirag Shah{1}, Aditya Karmarkar{2}, Xiaopeng Xu{2}
{1}GLOBALFOUNDRIES, INC., United States; {2}Synopsys, Inc., United States

<*Abstract*>
A novel simulation approach is developed to examine the stress evolution in the chip-to-package interconnect structures during the sequential IC Backend processes followed by packaging operation. Packaging induced stress in near-bump and BEOL level models is examined using the multi-level FEA methodology. Likewise, the Backend process induced stresses in the interconnect structures is analyzed using a sequential process simulation that looks into stress evolution of the BEOL structure as each metal-dielectric layer is being patterned. Finally, the cumulative impact of packaging induced stress and the BEOL process induced stress on the interconnect structures is examined to demonstrate the significance of this approach in performing a “design dependent” CPI risk analysis for BEOL interconnects.

16:40-17:10

4-3 ***INVITED - CPI Challenges in Advanced Si Technology Nodes***

C.S. Liu, H.P. Pu, C.S. Chen, H.Y. Tsai, C.H. Lee, M.J. Lii, Doug C.H. Yu
Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan

<*Abstract*>
The key chip-package-integration (CPI) challenges and solutions in the packaging and assembly of advanced Si technology nodes are reported. The key challenge of CPI due to the use of fragile extreme low-k (ELK) dielectric materials in the back-end-of-line (BEOL) layer has been resolved by optimizing bump structure and materials set including both the organic substrate and solder materials, along with process improvements for both Pb-free solder and Cu bump in flip chip packages.

17:10-17:35

4-4 ***A Simple Model-Base Prediction Method for Delamination Failures in Low-K/Cu Interconnects with Flip Chip Packages***

Jun Kawahara, Ippei Kume, Hirokazu Honda, Yoshitaka Kyougoku, Fuminori Ito, Masami Hane, Keiichirou Kata, Yoshihiro Hayashi
Renesas Electronics Corporation, Japan

<Abstract>
We proposed the model-based prediction method of the WB bump failure. The occurrence of the WB failure is able to be predicted by a simple evaluation function of the simulated strain energy referred to a proposed critical energy release rate Gc* of crack, which is defined by the fracture toughness Kc and the adhesion-strength of the low-k film Ka. The consideration of Ka becomes more accurate the prediction. This method gives us preliminary design guidelines on the bump pitch/structure or the interposer material/structure toward no WB failure quickly.

17:35-18:00

4-5 ***Tier-Independent Microfluidic Cooling for Heterogeneous 3D ICs with Nonuniform Power Dissipation***

Yue Zhang, Li Zheng, Muhannad Bakir
Georgia Institute of Technology, United States

<Abstract>
Embedded microfluidic cooling is considered a promising solution for heat removal in 3D ICs. This paper presents tier-independent microfluidic cooling in a 2-tier chip thermal testbed. Each tier has 4 segmented heaters emulating a simplified multicore processor. Tier-independent cooling is shown to reduce the pumping power by 37.5% by preventing over-cooling when an operating temperature is specified. Thermal coupling for 3D chips with liquid cooling is also discussed.