TECHNICAL SESSIONS

June 13, 2013

10:25-12:10

Session 2: Process integration I
Session Co-chairs:
Muhannad Bakir, Georgia Institute of Technology
Toshiaki Hasegawa, Sony

10:25-10:55

2-1 ***INVITED - Spanning the Spectrum of Interconnects: From Trenches of Double Patterning to System Level***

Nagaraj N. S.
University of Texas at Dallas, United States

<*Abstract*>
This talk covers the fascinating aspects of the whole spectrum of interconnects from trenches of silicon in nanometers to multi-millimeter long wires at system level and how common principles govern them. This talk starts at the silicon level, where double and triple patterning is becoming more common at lower level interconnects and these offer unique challenges and opportunities in manufacturability, variability and signal/power integrities. Then, it covers the CMP and inter-layer variation induced challenges and opportunities at global interconnects in silicon and expands to interposer and TSV aspects. This is followed by package and board level challenges and opportunities in manufacturability, electromagnetic interference and signal/power integrities. A concept of 'Interconnect Continuum' is introduced to show how viewing the whole spectrum in continuity helps in optimizing performance, power, cost and overall reliability.

10:55-11:20

2-2 ***Subtractive W Contact and Local Interconnect Co-Integration (CLIC)***

Fei Liu{2}, Benjamin Fletcher{2}, Eric Joseph{2}, Yu Zhu{2}, Jemima Gonsalves{2}, William Price{2}, Gregory Fritz{2}, Sebastian Engelmann{2}, Adam Pyzyna{1}, Zhen Zhang{1}, Cyril Cabral Jr{1}, Michael Guillorn{2}
{1}IBM T. J. Watson Re, United States; {2}IBM T. J. Watson Research Center, United States

<*Abstract*>
The resistivity of W interconnects deposited by physical vapor deposition (PVD) and chemical vapor deposition (CVD) is studied. The impacts of the deposition process and liner film stacks are explored. The results show acceptable resistivity for local interconnect (LI) applications with a linewidth down to 20nm and a wiring pitch down to 60nm. An integration scheme for combining a CVD W contact and local interconnect is explored as a means of providing a compact wiring solution with minimal impact on process complexity. The wiring concept is validated by integrating the local interconnects with trigate transistors.

11:20-11:45

2-3 ***CVD Mn-Based Self-Formed Barrier for Advanced Interconnect Technology***

Yong Kong Siew{2}, Nicolas Jourdan{2}, Yohan Barbarin{2}, Jerome Machillot{1}, Steven Demuynck{2}, Kristof Croes{2}, Jennifer Tseng{1}, Hua Ai{1}, J. Tang{1}, M. Naik{1}, P. Wang{1}, Murali Narasimhan{1}, M. Abraham{1}, Andrew Cockburn{1}, Jürgen Bömmels{2}, Zsolt Tőkei{2}
{1}Applied Materials, Belgium; {2}IMEC, Belgium

<*Abstract*>
CVD Mn-based self-formed barrier (SFB) has been evaluated and integrated for

reliability and RC delay assessment. Intrinsic TDDB lifetimes were extracted from planar capacitor measurement. A comparable lifetime as the TaN/Ta reference was obtained on SiO2 and porous low-k with a thin oxide liner. Good reliability performance was demonstrated after integration. Compared to conventional barrier, significant RC reduction (up to 45% at 40nm half pitch) and lower via resistance which become more beneficial upon scaling present CVD Mn-based SFB as an attractive candidate for future interconnect technology.

11:45-12:10

2-4 ***Reliable Integration of Robust Porous Ultra Low-k (ULK) for the Advanced BEOL Interconnect***

Kyu-Hee Han, Seungwook Choi, Tae Jin Yim, Seunghyuk Choi, Jongmin Baek, Sang Hoon Ahn, Nae-In Lee, Siyoung Choi, Ho-Kyu Kang, Es Jung
Samsung Electronics, Korea, South

<Abstract>
In order to address the increasing RC and reliability challenges at the advanced technology nodes, a new robust ULK was developed that incorporates the bridging carbon atoms (Si-[CH2]x-Si) in p-SiOCH matrix. Its elastic modulus and plasma damage resistance were improved more than 40% at the same dielectric constant than the commercially available ULK. These improvements are attributed to 80% higher atoms that exist in both Si-[CH2]x-Si and Si-CH3 structures with its pore size 23% smaller. Furthermore, its superb properties resulted in 3~4% capacitance reduction, and improvement of TDDB and EM TTF (time to failure) by 2 order and 2~3 times, respectively, on an advanced BEOL vehicle.

12:10-13:40 **Lunch**