IITC

2013 IEEE International Interconnect Technology Conference
June 13-15, 2013 Kyoto Research Park, Kyoto, Japan

TECHNICAL SESSIONS

June 13, 2013

09:00-09:10 Opening/ *Welcome and Introduction*

09:10-10:10

Session 1: Plenary Session

Session Co-chairs:
Shinichi Ogawa, AIST
Azad Naeemi, Georgia Institute of Technology
Andreas Klipp, BASF Electronic Materials

09:10-10:10

1-1 ***Keynote Presentation - Innovative Wafer-based Interconnect Enabling Advanced Packaging and Semiconductor Paradigm Shift***

Douglas Chen-Hua Yu, Senior Director, Integrated Interconnect and Package Division, R&D, Taiwan Semiconductor Manufacturing Co., Ltd.
Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan

<Abstract>
In semiconductor world, there is a new paradigm shift from chip-scaling to system-scaling to meet the ever-increasing electronic system demands in power saving, performance, and functionality (including memory bandwidth) increase, form factor improvement and cost reduction. This shift is also triggered by the growing concerns for industry to sustain Moore's Law. Innovations on wafer-based interconnect enable advanced packaging, that, in turn, enables system scaling and paradigm shift from transistor scaling. The innocations present in this speech include wafer-level-packaging (fan-in and fan-out), through-Si-via (3DIC and interposer) and ultra-thin Package-on-Package for both high performance and smart mobile applications. We also show that the industry can not only leverage wafer interconnect technologies, but also re-invent micro-electronics so that we can continue delivering more advanced systems, whether or not Moore's Law can be sustained.

10:10-10:25 Break

10:25-12:10

Session 2: Process integration I

Session Co-chairs:
Muhannad Bakir, Georgia Institute of Technology
Toshiaki Hasegawa, Sony Corp.

10:25-10:55

2-1 ***INVITED - Spanning the Spectrum of Interconnects: From Trenches of Double Patterning to System Level***

N. S. Nagaraj
University of Texas at Dallas, United States

<Abstract>
This talk covers the fascinating aspects of the whole spectrum of interconnects from trenches of silicon in nanometers to multi-millimeter long wires at system level and how common principles govern them. This talk starts at the silicon level, where double and triple patterning is becoming more common at lower level interconnects and these offer unique challenges and opportunities in manufacturability, variability and signal/power integrities. Then, it covers the CMP and inter-layer variation induced challenges and opportunities at global interconnects in silicon and expands to interposer and TSV aspects. This is followed by package and board level challenges and opportunities in

manufacturability, electromagnetic interference and signal/power integrities. A concept of 'Interconnect Continuum' is introduced to show how viewing the whole spectrum in continuity helps in optimizing performance, power, cost and overall reliability.

10:55-11:20

2-2 Subtractive W Contact and Local Interconnect Co-Integration (CLIC)

Fei Liu{2}, Benjamin Fletcher{2}, Eric Joseph{2}, Yu Zhu{2}, Jemima Gonsalves{2}, William Price{2}, Gregory Fritz{2}, Sebastian Engelmann{2}, Adam Pyzyna{1}, Zhen Zhang{1}, Cyril Cabral Jr{1}, Michael Guillorn{2}
{1}IBM T. J. Watson Re, United States; {2}IBM T. J. Watson Research Center, United States

<Abstract>
The resistivity of W interconnects deposited by physical vapor deposition (PVD) and chemical vapor deposition (CVD) is studied. The impacts of the deposition process and liner film stacks are explored. The results show acceptable resistivity for local interconnect (LI) applications with a linewidth down to 20nm and a wiring pitch down to 60nm. An integration scheme for combining a CVD W contact and local interconnect is explored as a means of providing a compact wiring solution with minimal impact on process complexity. The wiring concept is validated by integrating the local interconnects with trigate transistors.

11:20-11:45

2-3 CVD Mn-Based Self-Formed Barrier for Advanced Interconnect Technology

Yong Kong Siew{2}, Nicolas Jourdan{2}, Yohan Barbarin{2}, Jerome Machillot{1}, Steven Demuynck{2}, Kristof Croes{2}, Jennifer Tseng{1}, Hua Ai{1}, J. Tang{1}, M. Naik{1}, P. Wang{1}, Murali Narasimhan{1}, M. Abraham{1}, Andrew Cockburn{1}, Jürgen Bömmels{2}, Zsolt Tõkei{2}
{1}Applied Materials, Belgium; {2}IMEC, Belgium

<Abstract>
CVD Mn-based self-formed barrier (SFB) has been evaluated and integrated for reliability and RC delay assessment. Intrinsic TDDB lifetimes were extracted from planar capacitor measurement. A comparable lifetime as the TaN/Ta reference was obtained on SiO2 and porous low-k with a thin oxide liner. Good reliability performance was demonstrated after integration. Compared to conventional barrier, significant RC reduction (up to 45% at 40nm half pitch) and lower via resistance which become more beneficial upon scaling present CVD Mn-based SFB as an attractive candidate for future interconnect technology.

11:45-12:10

2-4 Reliable Integration of Robust Porous Ultra Low-k (ULK) for the Advanced BEOL Interconnect

Kyu-Hee Han, Seungwook Choi, Tae Jin Yim, Seunghyuk Choi, Jongmin Baek, Sang Hoon Ahn, Nae-In Lee, Siyoung Choi, Ho-Kyu Kang, Es Jung
Samsung Electronics, Korea, South

<Abstract>
In order to address the increasing RC and reliability challenges at the advanced technology nodes, a new robust ULK was developed that incorporates the bridging carbon atoms (Si-[CH2]x-Si) in p-SiOCH matrix. Its elastic modulus and plasma damage resistance were improved more than 40% at the same dielectric constant than the commercially available ULK. These improvements are attributed to 80% higher atoms that exist in both Si-[CH2]x-Si and Si-CH3 structures with its pore size 23% smaller. Furthermore, its superb properties resulted in 3~4% capacitance reduction, and improvement of TDDB and EM TTF (time to failure) by 2 order and 2~3 times, respectively, on an advanced BEOL vehicle.

12:10-13:40 **Lunch**

13:40-15:25

Session 3: Reliability
Session Co-chairs:
Larry Zhao, GlobalFoundries
Shinichi Ogawa, AIST

13:40-14:10

3-1 ***INVITED - The Electromigration Short " Length Effect and Its Impact on Circuit Reliability***

Anthony Oates
TSMC, Taiwan

<Abstract>
The short-length effect, whereby electromigration is eliminated due a mechanical stress gradient induced backflow, has long been recognized as a fundamental facet of electromigration failure of IC interconnects. More recently, the short " length effect has been shown to have a profound impact on the statistics of electromigration failure. In this presentation we will review recent experimental studies of short-length effects in Cu/low-k interconnects, and the statistical modeling of failure distributions. The most significant finding is that failure can occur at average current densities below the critical value implied by the critical current density " length product. This results from manufacturing variability in conductor geometry and in the critical current density itself. On this basis we can accurately model failure distributions as a function of stress variables, conductor geometry, and presence of reservoirs. We also propose a new reliability extrapolation procedure to account for short-length effects.

14:10-14:35

3-2 ***Critical Initial Void Growth for Electromigration: Stress Modeling and Multi-Link Statistics for Cu/Low-K Interconnects***

Zhuojie Wu{2}, Linjun Cao{2}, Jay Im{2}, Ki-Don Lee{1}, Paul Ho{2}
{1}Texas Instruments, United States; {2}The University of Texas at Austin, United States

<Abstract>
This paper investigated the initial void growth that determines the electromigration failure time for Cu/low-k interconnects. A method to derive the initial void growth rate prior to line failure by analyzing the resistance traces was developed. The statistical data from multi-linked structures show a linear relationship between the void growth rates before and after failure. An extended the Korhonen model was developed taking into account the stress effect on void growth for Cu interconnects. The model was able to account for the observed EM statistics, thus suggesting that the effect of stress should be included for EM lifetime extrapolation.

14:35-15:00

3-3 ***Void Nucleation and Growth During Electromigration in 30 nm Wide Cu Lines: Impact of Different Interfaces on Failure Mode***

Tomoyuki Kirimura{1}, Kristof Croes{2}, Yong Kong Siew{2}, Kris Vanstreels{2}, Piotr Czarnecki{2}, Zaid El-Mekki{2}, Marleen van der Veen{2}, Dries Dictus{3}, Alex Yoon{3}, Artur Kolics{3}, Juergen Boemmels{2}, Zsolt Tokei{2}
{1}Fujitsu Semiconductor Europe, Belgium; {2}Imec, Belgium; {3}Lam Research Corporation, United States

<Abstract>
We investigate void nucleation and growth during electromigration (EM) in 30 nm half pitch Cu lines. Diffusion interfaces are varied by using SiCN cap or a CoWP

metal cap, and by tuning the thickness of barrier metal. The EM failure modes are dependent on the cap materials but not on the barrier thickness. For CoWP capped Cu lines, since Co can diffuse into the interface between the barrier metal and Cu, both Cu diffusivities at the cap and barrier interfaces are suppressed. A CoWP cap is beneficial to EM for advanced interconnects where thinner barrier metals are required.

15:00-15:25

3-4 ***AC and Pulsed-DC Stress Electromigration Failure Mechanisms in Cu Interconnects***

Ming-Hsien Lin, Anthony S. Oates
Taiwan Semiconductor Manufacturing Company. Ltd.,, Taiwan

<Abstract>
The effects of AC and pulsed-DC (PDC) waveforms on electromigration failure distributions in Cu / low-k interconnects are examined. No failures are observed with a 1MHz pure AC stress, consistent with average current density controlled kinetics and complete recovery of damage during current reversal. Failure distributions with PDC stress are consistent with a degradation process that is determined by average current density and void growth kinetics.

15:25-15:45 **Break**

15:45-18:00

Session 4: Packaging
Session Co-chairs:
Takeshi Furusawa, Renesas Electronics
Tomoji Nakamura, Fujitsu Labs

15:45-16:15

4-1 ***INVITED - Experimental Analysis of Mechanical Stresses and Material Properties in Multi-Layer Interconnect Systems by fibDAC***

Dietmar Vogel, Ellen Auerswald, Bernd Michel, Sven Rzepka
Fraunhofer ENAS, Germany

<Abstract>
The paper presents a new stress measurement method on base of stress relief caused by local material removal with ion milling in FIB equipment. Stress relief deformations extracted from SEM micrographs by means of digital im-age correlation allow the determination of stresses, as well as to estimate Young's modulus on the position of ion milling. The paper gives an introduction into the method. The feasibility to extract local stresses in multilayer stacks, both in lateral direction and in depth, is discussed in more detail.

16:15-16:40

4-2 ***Modeling of Interconnect Stress Evolution During BEOL Process and Packaging***

Chirag Shah{1}, Aditya Karmarkar{2}, Xiaopeng Xu{2}
{1}GLOBALFOUNDRIES, INC., United States; {2}Synopsys, Inc., United States

<Abstract>
A novel simulation approach is developed to examine the stress evolution in the chip-to-package interconnect structures during the sequential IC Backend processes followed by packaging operation. Packaging induced stress in near-bump and BEOL level models is examined using the multi-level FEA methodology. Likewise, the Backend process induced stresses in the interconnect structures is analyzed using a sequential process simulation that looks into stress

evolution of the BEOL structure as each metal-dielectric layer is being patterned. Finally, the cumulative impact of packaging induced stress and the BEOL process induced stress on the interconnect structures is examined to demonstrate the significance of this approach in performing a "design dependent" CPI risk analysis for BEOL interconnects.

16:40-17:10

4-3 ***INVITED - CPI Challenges in Advanced Si Technology Nodes***

C.S. Liu, H.P. Pu, C.S. Chen, H.Y. Tsai, C.H. Lee, M.J. Lii, Doug C.H. Yu
Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan

<Abstract>

The key chip-package-integration (CPI) challenges and solutions in the packaging and assembly of advanced Si technology nodes are reported. The key challenge of CPI due to the use of fragile extreme low-k (ELK) dielectric materials in the back-end-of-line (BEOL) layer has been resolved by optimizing bump structure and materials set including both the organic substrate and solder materials, along with process improvements for both Pb-free solder and Cu bump in flip chip packages.

17:10-17:35

4-4 ***A Simple Model-Base Prediction Method for Delamination Failures in Low-K/Cu Interconnects with Flip Chip Packages***

Jun Kawahara, Ippei Kume, Hirokazu Honda, Yoshitaka Kyougoku, Fuminori Ito, Masami Hane, Keiichirou Kata, Yoshihiro Hayashi
Renesas Electronics Corporation, Japan

<Abstract>

We proposed the model-based prediction method of the WB bump failure. The occurrence of the WB failure is able to be predicted by a simple evaluation function of the simulated strain energy referred to a proposed critical energy release rate Gc* of crack, which is defined by the fracture toughness Kc and the adhesion-strength of the low-k film Ka. The consideration of Ka becomes more accurate the prediction. This method gives us preliminary design guidelines on the bump pitch/structure or the interposer material/structure toward no WB failure quickly.

17:35-18:00

4-5 ***Tier-Independent Microfluidic Cooling for Heterogeneous 3D ICs with Nonuniform Power Dissipation***

Yue Zhang, Li Zheng, Muhannad Bakir
Georgia Institute of Technology, United States

<Abstract>

Embedded microfluidic cooling is considered a promising solution for heat removal in 3D ICs. This paper presents tier-independent microfluidic cooling in a 2-tier chip thermal testbed. Each tier has 4 segmented heaters emulating a simplified multicore processor. Tier-independent cooling is shown to reduce the pumping power by 37.5% by preventing over-cooling when an operating temperature is specified. Thermal coupling for 3D chips with liquid cooling is also discussed.

June 14, 2013

09:00-10:20

Session 5: Unit Process I
Session Co-chairs:
Naoya Inoue, Renesas Electronics
Ivo Raaijmakers, ASM International nv

09:00-09:30

5-1 ***INVITED - Damage Free Cryogenic Etching of Ultra Low-k Materials***

Mikhail R. Baklanov{1}, Liping Zhang{1}, Rémi Dussart{2}, Jean-François de Marneffe{1}
{1}IMEC, Belgium, {2}GREMI/Université d'Orléans, France

<Abstract>
Cryogenic etching was applied to porous organosilicate (OSG) films. Plasma-induced damage was reduced due to the protective effect of etch by-products condensed in pores of low-k materials. Almost no carbon depletion was observed when the wafer temperature is below a certain critical level. Most of experiments were carried out with SF_6 plasma. The addition of SiF_4/O_2 into the gas discharge allows a further reduction of plasma-induced damage by formation of a SiO_xF_y passivation layer.

09:30-09:55

5-2 ***Extremely Non-Porous Ultra-Low-K SiOCH (k=2.3) with Sufficient Modulus (>10 GPa), High Cu Diffusion Barrier and High Tolerance for Integration Process Formed by Large-Radius Neutral-Beam Enhanced CVD***

Yoshiyuki Kikuchi{2}, Akira Wada{1}, Seiji Samukawa{1}
{1}Institute of Fluid Science, Tohoku University, Japan; {2}Tokyo Electron Technology and Development Institute, Japan

<Abstract>
We developed a practical large-radius neutral beam enhanced CVD with a dimethoxy tetramethy ldisiloxane (DMOTMDS) to form low-k SiOCH film on 8-inch Si wafers. We fabricated extremely non-porous film with an ultra-low k-value of 2.3 and a sufficient modulus (>10 GPa). This particular film did not show any damage from the oxygen plasma and acid or alkali solutions used in the fabrication process. Furthermore, the dense film almost completely resisted Cu diffusion into the film during thermal annealing.

09:55-10:20

5-3 ***Macroscopic and microscopic interface adhesion strength of copper damascene interconnects***

Nobuyuki Shishido{4}, Shoji Kamiya{4}, Chuantong Chen{4}, Hisashi Sato{4}, Kozo Koiwa{4}, Masaki Omiya{3}, Masahiro Nishida{4}, Takashi Suzuki{1}, Tomoji Nakamura{1}, Takeshi Nokuo{2}, Toshiaki Suzuki{2}
{1}Fujitsu Laboratories Ltd., Japan; {2}JEOL Ltd., Japan; {3}Keio University, Japan; {4}Nagoya Institute of Technology, Japan

<Abstract>
Macroscopic and microscopic adhesion strength of damascene interconnects was investigated by evaluating local strength through delaminating different scales of adhesion area under SEM observation. Macroscopic strength obtained by the areas larger than the copper grain was almost constant after considering the macroscopic plastic deformation. However, microscopic strength obtained by the areas smaller than the copper grain spread around the macroscopic strength and was highly sensitive to the copper grain structure, especially the grain boundary.

10:20-10:40 **Break**

10:40-12:00

Session 6: Unit Process II
Session Co-chairs:
Ivo Raaijmakers, ASM International nv
Naoya Inoue, Renesas Electronics

10:40-11:10

6-1 ***INVITED - Grain boundary and surface scattering in interconnect metals***

Kevin Coffey{2}, Katayun Barmak{1}, Tik Sun{2}, Andrew Warren{2}, Bo Yao{2}
{1}Columbia University, United States; {2}University of Central Florida, United States

<Abstract>
The talk addresses the classical size effect in interconnect metals and presents our work on understanding and quantifying the contributions of grain boundary and surface scattering to the observed resistivity increase. Experimental studies of both Cu and W films will be described, including the development of improved metrology techniques for nanoscale metals characterization. The extent to which the experimental data supports the theoretically expected interactions between surface and grain boundary scattering mechanisms will also be discussed.

11:10-11:35

6-2 ***Deposition Behavior and Substrate Dependency of ALD MnOx Diffusion Barrier Layer***

Kenji Matsumoto{3}, Kaoru Maekawa{1}, Hiroyuki Nagai{3}, Junich Koike{2}
{1}TEL Technology Center, America, LLC., United States; {2}Tohoku University, Japan; {3}Tokyo Electron Ltd., Japan

<Abstract>
We investigated the possibility of applying an ALD method to form a Cu diffusion barrier layer of MnOx in an attempt to develop a deposition process which would not be influenced by absorbed water in a substrate. The MnOx formed by ALD using (EtCp)2Mn and H2O had the following features. (1) Capability of thickness control of the MnOx layer by changing the ALD cycle number. (2) Capability of the ALD-MnOx formation on low-k dielectrics by surface modification. (3) Good adhesion of the Cu/ALD-MnOx/SiOCH structure showing a fracture toughness of 0.3 MPam1/2. (4) Good diffusion barrier property for the thickness of over 1 nm. (5) Minimizing via resistance increase accompanied by the formation of MnOx on Cu.

11:35-12:00

6-3 ***Pore-Sealing Process Initiated by Self-Assembled Layer for Extreme Low-K SiOCH (k=2.0)***

Akiko Kobayashi, Dai Ishikawa, Kiyohiro Matsushita, Nobuyoshi Kobayashi
ASM, Japan

<Abstract>
A pore sealing process by Plasma-enhanced ALD has been developed, which enabled simultaneous restoration and pore-sealing film formation on damaged low-k film with k = 2.0. The precursor adsorbed preferentially at OH termination on the low-k surface to form self-assembled SiOC layer, which simultaneously recovered low-k damage. It is suggested that the SiOC layer narrowed the pore opening at the low-k surface, and was followed by hermetic SiCN layer formation by PEALD. The current process will pave the way for enabling extremely thin diffusion barrier <2nm at 1X nm node Cu interconnect.

12:00-13:30 Lunch

13:30-15:00 Session 7: Poster Session

7-1 ***Early Screening Method of Chip-Package Interaction for Multi-Layer Cu/Low-K Structure Using High Load Indentation Test***

Tatsuya Usami, Tomoyuki Nakamura, Iwao Yashima
Renesas Electronics Corporation, Japan

<Abstract>
We have developed High Load Indentation test as a novel early screening method of Chip-Package Interaction for multi-layer Cu/Low-k interconnects structure with bumps. In this study, by using HiLI test, we evaluated a lower fracture toughness SiCOH, a thicker under bump metallization and a plasma-damaged polyimide around these bumps, whose white bump failures relatively tend to occur compared to the standard structure. We found that both these in-situ load profiles and observations after the test corresponded with these white bump failures. In addition, we compared between a polished bump structure and an un-polished bump one by the test.

7-2 ***Early Failure of Short-Lead Metal Line and its Em Characterization with Wheatstone Bridge Structure in Advanced Cu/ULK BEOL Process***

Tae-Young Jeong, Sari Windu, Dong-Cheon Baek, Jinseok Kim, Kyuho Tak, Miji Lee, Hyunjun Choi, Sangwoo Pae, Jongwoo Park
Samsung Electronics, Korea, South

<Abstract>
Early failure of the short-lead metal EM (Electromigration) is investigated. Applying Wheatstone bridge (WSB) test structure and 3-parameter lognormal distribution enables to reduce sample size and time-to-fail (TTF) variation governed by early fails causing a poor standard deviation, EM lifetime is accurately predicted and improved by ~280x. In particular, EM TTF at lower percentiles can be well represented by 3-parameter lognormal. With respect to physical aspects of void, EM behaviors of the short-lead and long-lead metal line are addressed based on experimental results compared with Monte-Carlo simulations to support the Blech's back-stress effects.

7-3 ***Redundancy Method to Assess Electromigration Lifetime in Power Grid Design***

Boukary Ouattara{3}, Lise Doyen{2}, David Ney{2}, Habib Mehrez{1}, Pirouz Bazargan-Sabet{1}, Franck Lionel Bana{2}
{1}Laboratory of Computer Sciences, Paris 6 (LIP6), France; {2}STMicroelectronics, France; {3}STMicroelectronics/Laboratory of Computer Sciences, Paris 6 (LIP6), France

<Abstract>
The tendency of semiconductor market to increase component density in small chip leads to reliability issues such as Electromigration (EM). This phenomenon becomes critical in deep submicron design technology. In this paper we assess chip power grid lifetimes by taking into account redundant paths contribution in case of EM degradation. The application of this method for wire lifetime validation of a 32nm microprocessor has reduced significantly wires susceptible to EM given by simulation tools.

7-4 ***Compact Modeling and Optimization of Fine-Pitch Interconnects for Silicon Interposers***

Vachan Kumar, Li Zheng, Muhannad Bakir, Azad Naeemi
Georgia Institute of Technology, United States

<Abstract>
This paper presents the first optimization methodology for silicon interposer interconnect technology. The dimensions of these fine-pitch interconnects are roughly a few microns, because of which they can neither be treated as on-chip RC interconnects, nor as conventional off-chip interconnects. 3D extraction tools can provide an accurate estimate of the circuit parameters, but they prove to be very slow and tedious for design space exploration and optimization. Thus, the novel analytical models developed here for the frequency dependent resistance of fine-pitch interconnects are essential to efficiently optimize these interconnects. The error in the model is shown to be less than 15% for interconnect dimensions and frequency range of interest. The analytical models developed are then used to optimize the data-rate and cross-sectional dimensions to maximize the bandwidth-density and minimize the energyper-bit, simultaneously.

7-5 ***Low Temperature Bonding of Sn/in-Cu Interconnects for Three-Dimensional Integration Applications***

Ruoh-Ning Tzeng{2}, Yan-Pin Huang{2}, Yu-San Chien{2}, Ching-Te Chuang{2}, Wei Hwang{2}, Jin-Chern Chiou{2}, Ming-Shaw Shy{1}, Kuan-Neng Chen{2}, Teu-Hua Lin{1}, Kou-Hua Chen{1}, Chi-Tsung Chiu{1}, Ho-Ming Tong{1}
{1}Advanced Semiconductor Engineering Group, Taiwan; {2}Department of Electronics Engineering, National Chiao Tung University, Taiwan

<Abstract>
A low temperature bonding technology of Sn/In composite solder bonded to Cu interconnect is proposed and investigated. The intermetallic compounds formed in the bonded interconnects can survive well in the following process. The Sn/In-Cu interconnects bonded at low temperature all exhibit excellent electrical performance and high resistance to multiple current stressing, showing a great potential in 3D applications.

7-6 ***Thin Nickel Films Growth Using Plasma Enhanced Atomic Layer Deposition from 2-methylallyl N,N'-diisopropylacetamidinate Nickel(II)***

Jiro Yokota{1}, Clement Lansalot{2}, Changhee Ko{1}
{1}Air Liquide Laboratories, Japan; {2}Air Liquide Laboratories Korea, Korea, South

<Abstract>
2-methylallyl-N,N'-diisopropylacetamidinate nickel(II) is a promising precursor for the deposition of pure nickel film to be later used in the silicidation process. High purity, high deposition rate, low resistivity of the film and good step coverage were successfully confirmed for the deposition of pure metal nickel films.

7-7 ***Annealing Effect on the Structure Characteristics of Nano-Scale Damascene Copper Lines***

Tatyana Konkova{1}, Sergey Mironov{2}, Yiqing Ke{1}, Jin Onuki{1}
{1}Ibaraki University, Japan; {2}Tohoku University, Japan

<Abstract>
High-resolution electron backscatter diffraction (EBSD) technique was applied for systematic and detailed study of grain structure and texture changes in various microstructural regions of nano-scale damascene copper lines after annealing in a wide temperature range of 200-500C. To ensure reliability of the obtained results, large EBSD maps including several thousand grains were obtained in each case. Above 200 C, the grain structure was established to be surprisingly stable in both the overburden layer as well as within the lines. The grain growth in the lines was supposed to be suppressed by pinning effect of second-phase particles entrapped during electrodeposition process.

7-8 ***Endpoint Detection Using Optical Emission Spectroscopy in TSV Fabrication***

Ja Myung Gu{1}, Paragkumar Thadesar{1}, Ashish Dembla{1}, Sang Jeen Hong{2}, Muhannad Bakir{1}, Gary May{1}
{1}Georgia Institute of Technology, United States; {2}Myongji University, Korea, South

<Abstract>
A hybrid partial least squares-support vector machine (PLS-SVM) model of optical emission spectroscopy data is proposed and successfully demonstrated to predict the endpoint detection of through silicon vias (TSVs) etched using the Bosch process. Accurate results are shown for TSVs with diameters of 80 μm and 25 μm.

7-9 ***MOCVD-Cobalt Liner Integration for Sub-30 nm Copper Metallization***

Lukas Gerlich{1}, Marcus Wislicenus{1}, Robert Krause{1}, Boris Vasilev{1}, Axel Preuße{2}, Romy Liske{1}
{1}Fraunhofer CNT, Germany; {2}GLOBALFOUNDRIES, Dresden, Germany

<Abstract>
For Cu-metallization Co was deposited as a novel liner in a MOCVD process on a conventionally deposited (PVD) barrier layer. Besides the electrical tests on short loop wafers the filling behavior was examined with TEM-EDX in test structures to characterize sidewall coverage. The contact resistances measured in sub-30 nm structures for Co-liners without Cu-seed showed competitive data to the conventionally used copper seeded counterpart. For copper seeded cobalt liner the contact resistance could be improved by adjustment of the TaN underlayer.

7-10 ***Beam-Substrate Interaction During Tungsten Deposition by Helium Ion Microscope***

Shinichi Ogawa, Kazuyuki Kohama, Tomohiko Iijima, Misa Hayashida
National Institute of Advanced Industrial Science and Technology(AIST), Japan

<Abstract>
We deposited tungsten-based pillars on about 300 nm-thick carbon and silicon substrates by a helium ion microscope using W(CO)6 as a gaseous precursor. We then investigated beam-induced damage to the substrates correlated with both pillar growth rate and material type of substrates. Faster pillar growth reduced the substrate damage because the pillars shielded the substrates from the incident beam, resulting in a low-damage process. On the other hand, the Si substrate was significantly damaged by the incident beam compared with the carbon substrates. This is because stopping cross-section of 30-keV helium ion in silicon is about 1.5 times higher than that in carbon. The incident helium ions were considered to induce the substrate damage in the process of losing energy in the substrates.

7-11 ***Development and Evaluation of a-SiC:H Films Using a dimethylsilacyclopentane Precursor As a Low-K Cu Capping Layer***

Els Van Besien, Cong Wang, Patrick Verdonck, Arjun Singh, Yohan Barbarin, Jean-François de Marneffe, Kris Vanstreels, Hilde Tielens, Marc Schaekers, Mikhail R. Baklanov, Sven Van Elshocht
IMEC, Belgium

<Abstract>
Scaling of the Cu interconnect structures requires Cu capping layers with an increasingly lower dielectric constant that still have adequate Cu and moisture barrier properties. In this work, we study the plasma enhanced chemical vapour (PE-CVD) deposition of amorphous silicon carbide films using dimethyl silacyclopentane (DMSCP) as a precursor, resulting in the incorporation of Si-(CH2)n-Si bridges. The effect of process parameters on film characteristics like dielectric constant, mass density, and leakage behaviour is investigated, as well as

their relation with the chemical bonding structure. Finally, Cu barrier properties and hermeticity are evaluated.

7-12 ***Stress Reduction Induced by Bosch Scallops on an Open TSV Technology***

Anderson Singulani, Hajdin Ceric, Erasmus Langer
Technical University of Vienna, Austria

<Abstract>
Through Silicon Via (TSV) is a lead topic in interconnects and 3D integration research, mainly due to numerous anticipated advantages. However, several challenges must still be overcome if large scale production is to be achieved. In this work, we have studied effects of Bosch scallops concerning mechanical reliability for a specific TSV technology. We identified that the presence of scallops on the TSV wall modifies the stress distribution. The achieved results support experiments and give a better insight into the influence of scallops in an open TSV.

7-13 ***Fabrication and Electrical Characterization of 5x50um Through Silicon Vias for 3D Integration***

Bharat Bhushan, Minrui Yu, John Dukovic, Loke Yuen Wong, Aksel Kitowski, Mun Kyu Park, John Hua, Shwetha Bolagond, Anthony C-T Chan, Chin Hock Toh, Arvind Sundarrajan, Niranjan Kumar, Sesh Ramaswami
Applied Materials, United States

<Abstract>
We present fabrication, electrical characterization, and metrology analysis results of 5×50um TSVs for 3D integration. Specifically, electrical performance of blind TSVs is evaluated by capacitance-voltage (CV) and current-voltage (IV) measurements. Important electrical parameters such as oxide capacitance, minimum TSV capacitance, leakage current, and breakdown voltage are extracted and show good results. The capacitance values also closely match model predictions. The electrical testing data are further verified with a variety of materials analysis techniques.

7-14 ***Electrical Properties of Multilayer Graphene Interconnects Prepared by Chemical Vapor Deposition***

Masayuki Katagiri, Hisao Miyazaki, Yuichi Yamazaki, Li Zhang, Takashi Matsumoto, Makoto Wada, Akihiro Kajita, Tadashi Sakai
Low-power Electronics Association & Project (LEAP), Japan

<Abstract>
We fabricate multilayer graphene interconnects with 100-nm-class line widths. Multilayer graphene is grown on a Ni catalyst layer using remote plasma-enhanced chemical vapor deposition (CVD) at a low temperature of 600 °C and transferred onto a SiO_2/Si substrate after exfoliation from the Ni layer. The sheet resistance of the CVD graphene interconnects is as low as 500 Ω/sq. The temperature dependence of resistance reveals that the CVD graphene exhibits half-metallic transport properties.

7-15 ***Advanced Nanostructured Materials Applied in Nanoelectronics***

Hui Lin Chang, Waylon Mcguigan
National Chiao Tung Univ, Taiwan

<Abstract>
A systematic work of random oriented SiCN tubes, nanowire/conical rod and 2-D graphite/seaweed structures are covered and their corresponding properties have been reached in this study. The growth mechanism and electronic properties of nanostructured materials have been addressed. The development of nanostructured materials is crucial in enhancing emerging devices application.

7-16 ***Numerical Simulations of High Heat Dissipation Technology in LSI 3-D Packaging Using Carbon Nanotube Through Silicon via (CNT-TSV) and Thermal Interface Material (CNT-TIM)***

Teppei Kawanabe{1}, Akio Kawabata{2}, Tomo Murakami{2}, Mizuhisa Nihei{2}, Yuji Awano{1}
{1}Keio University, Japan; {2}National Institute of Advanced Industrial Science and Technology, Japan

<Abstract>
We report numerical simulations of heat dissipation properties of nano-carbon through silicon via (TSV), thermal interface material (TIM), and chip package towards a high power heat dissipation LSI 3-D packaging. By using vertically aligned multi-walled CNTs (MWNTs) as both TSV and TIM materials and graphite as chip package, a boundary temperature just under a heat source decreased 40.8K in total, comparing to that using conventional materials. This result suggests superior heat dissipation properties of nano-carbon 3-D packaging.

7-17 ***Development of Sputtering Technology of Ta2O5/TaOx Stacked Film for ReRAM Mass-Production***

Natsuki Fukuda, Kazunori Fukuju, Yutaka Nishioka, Koukou Suu
ULVAC, Inc., Japan

<Abstract>
This paper deals with development of sputtering technology of Ta2O5/TaOx stacked film for ReRAM mass-production. Thickness of TaOx film deposited by sputtering process is possible to obtain with good uniformity. However, if a high deposition rate is required for mass production, it is very difficult to obtain good controllability and uniformity of TaOx film. These problems affect the switching characteristics of the ReRAM. In order to solve these problems, sputtering tool and process for ReRAM mass-production are developed. We report the result of TaOx film with good resistance uniformity and controllability and deposition stability without low deposition rate. Moreover, switching characteristics of Pt/Ta2O5/TaOx/Pt-ReRAM-cells are evaluated.

15:00-16:20

Session 8: 3D Integration I

Session Co-chairs:
Azad Naeemi, Georgia Institute of Technology
Kenichi Takeda, Hitachi

15:00-15:30

8-1 ***INVITED - Reliability Challenges of Through-Silicon-Via (TSV) Stacked Memory Chips for 3-D Integration: from Transistors to Packages***

Ho-Young Son, Woong-Sun Lee, Seung-Kwon Noh, Min-Suk Suh, Jae-Sung Oh, Nam-Seog Kim
SK Hynix, Korea, South

<Abstract>
Recently, three-dimensional stacked chip package using through-silicon vias (TSVs) is a major paradigm which leads the transition of semiconductor technology from 2-D to 3-D IC in the electronic industry. However, lots of reliability concerns lie in the developing stage and we should clear away doubtful suspicion prior to mass production of 3-D stacked chip package. In this paper, an overview of reliability issues of 3-D TSV integration is introduced dividing into three categories: zero-level reliability of FEOL (front-end of the-line) such as transistors and capacitors, 1st level of BEOL (back-end of the-line) metallization and TSV interconnections, and 2nd level of micro-bumps of stacked chip interfaces. This paper describes the essential scope of the reliability challenges in 3-D IC packaging technology by dealing with reliability issues from transistor-level of the memory device to package micro-bump level of chip-to-chip interconnections.

15:30-15:55

8-2 ***Impact of Material and Microstructure on Thermal Stresses and Reliability of Through-Silicon via (TSV) Structures***

Tengfei Jiang{3}, Suk-Kyu Ryu{1}, Jay Im{3}, Ho-Young Son{2}, Nam-Seog Kim{2}, Rui Huang{3}, Paul Ho{3}
{1}Applied Materials Inc, United States; {2}SK Hynix Inc, Korea, South; {3}University of Texas at Austin, United States

<Abstract>
Thermal stresses and microstructures of two TSV structures with different fabrication conditions have been investigated using the precision wafer curvature and synchrotron x-ray microdiffraction methods, providing the first direct observation of local plasticity in the TSVs. Microstructure studies by EBSD, chemistry analysis by TOF-SIMS and nanoindentation measurements were also conducted. Results from this study show that the electroplating chemistry directly affects the Cu microstructure, which in turn controls stress relaxation and build-up of the residual stress during thermal cycling. The implications on via extrusion and device keep-out zone (KOZ) are discussed.

15:55-16:20

8-3 ***Investigations on Partially Filled HAR TSVs for MEMS Applications***

Lutz Hofmann, Ina Schubert, Knut Gottfried, Stefan E. Schulz, Thomas Gessner
Fraunhofer ENAS, Germany

<Abstract>
This paper presents technological aspects for the vertical integration of MEMS Devices using HAR-TSV. For considerations of stress reduction the TSVs were only partially filled with copper. A comparison was made to ring shaped TSVs (i.e. copper ring with silicon core). Two approaches regarding the way of TSV implementation (before and after wafer bonding/ thinning, resp.) are discussed, concerning process ability and yield aspects. Electrical measurement yield 11 mΩ; for a single TSV and 76 mΩ; for a 4-point TSV-chain (incl. RDL).

16:20-16:40 Break

16:40-18:00

Session 9: Novel Materials & Process I

Session Co-chairs:
Mehul Naik, AMAT
Muhannad Bakir, Georgia Institute of Technology

16:40-17:10

9-1 ***INVITED - Interconnects with Single Conjugated Polymers***

Yuji Okawa{1}, Swapan K. Mandal{1},{2}, Marina Makarova{1}, Masakazu Aono{1}
{1}National Institute for Materials Science (NIMS), Japan; {2}Visva-Bharati University, India

<Abstract>
In order to fabricate a single-molecule electronic circuit, we have to develop a viable method for wiring each functional molecule. The best way to reduce the width of wires to that of single molecules is to connect the molecules with conductive organic polymers. We found before that a stimulation with the probe tip of a scanning tunneling microscope (STM) could initiate a chain polymerization of diacetylene compound. As a result, we could fabricate a single conjugated polydiacetylene chain at designated positions. Based on these previous studies, here we report a novel method for single molecular interconnects, which we call “chemical soldering.” Since the front edge of chain polymerization necessarily has a reactive chemical species, when the chain propagation encounters an adsorbed single functional molecule, a covalent bond is formed spontaneously.

17:10-17:35

9-2 A 0.9um Pixel Size Image Sensor Realized by Introducing Organic Photoconductive Film Into the BEOL Process

Shunsuke Isono, Tetsuo Satake, Takashi Hyakushima, Kenji Taki, Ryota Sakaida, Shinji Kishimura, Shuji Hirao, Kotaro Nomura, Naoki Torazawa, Makoto Tsutsue, Tetsuya Ueda
Panasonic Corporation, Japan

<Abstract>

A stacked image sensor with a 0.9 um pixel size fabricated by using organic photoconductive film (OPF) was realized. It is the first trial to introduce an active material, that is, an organic semiconductor into the BEOL process. This pixel structure is fabricated by using a standard 45 nm BEOL process. However, after OPF deposition, it is essential to restrict the thermal budget and to avoid oxygen, moisture, and plasma irradiation. By controlling the above conditions, a demonstration of a stacked image sensor with OPF, which has high sensitivity, high saturation charge, and a wide incident light angle, was successfully performed.

17:35-18:00

9-3 Origin of Large Contact Resistance in Organic Field-Effect Transistors

Takeo Minari, Chuan Liu
NIMS, Japan

<Abstract>

The large contact resistance (RC) in organic field-effect transistors (OFET) is one of the main limitation factors which prevent the reliable operation and further reduction in device dimensions. In this paper, we report dependence of the RC on the gate dielectric materials, which means that the density of charge traps in access region (from contact to channel) of devices plays a primary role for the large RC rather than energy mismatch between Fermi level of the metal electrode and valence band level of an organic semiconductor. Based on the finding, we fabricated top-gate OFET devices, the structure of which minimizes access region resistance. Very low RC of below 0.1 kƒÇ cm was successfully achieved in the top-gate OFETs. A field-effect mobility of 8.3 cm2/V s and near zero threshold voltage were obtained in top-gate devices based on dioctylbenzothienobenzothiophene.

June 15, 2013

09:00-10:20

Session 10: Process Integration II

Session Co-chairs:
Nae-In Lee, Samsung Electronics Co., Ltd.
Susumu Matsumoto, Panasonic Corp.

09:00-09:30

10-1 ***INVITED - 48nm pitch Cu Dual-Damascene Interconnects using Self Aligned Double Patterning Scheme***

Shyng-Tsong Chen{2}, Tae-Soo Kim{3}, Seo-woo Nam{1}, Neal Lafferty{2}, Chiew-Seng Koay{2}, Nicole Saulnier{2}, Wenhui Wang{1}, Yongan Xu{2}, Benjamin Duclaux{4}, Yann Mignot{4}, Marcy Beard{2}, Yunpeng Yin{2}, Hosadurga Shobha{2}, Oscar Van der Straten{2}, Ming He{1}, James Kelly{2}, Matthew Colburn{2}, Terry Spooner{2}
{1}Global Foundries, United States; {2}IBM, United States; {3}Samsung Electronics, United States; {4}STMicroelectronics, United States

<Abstract>
For sub-64nm pitch interconnects build, it is beneficial to use Self Aligned Double Patterning (SADP) scheme for line level patterning. Usually a 2X pitch pattern was printed first, followed by a Sidewall Image Transfer (SIT) technique to create the 1X pitch pattern. A block lithography process is then used to trim this pattern to form the actual designed pattern. In this paper, 48nm and 45nm pitch SADP build will be used as examples to demonstrate the SADP patterning scheme. General discussions about this patterning scheme will be provided including: 1) the process flow of this technique, 2) benefits of the technique vs. pitch split approach, 3) the design impact and limitation, and 4) the extendability to smaller line pitch build.

09:30-09:55

10-2 ***UV Cure Impact on Robust Low-K with Sub-nm Pores and High Carbon Content for High Performance Cu/Low-K BEOL Modules***

Naoya Inoue{3}, Fuminori Ito{3}, Hosadurga Shobha{2}, Stephen Gates{2}, Todd Ryan{1}, Kumar Virwani{2}, Nancy Klymko{2}, A. Madan{2}, L. Tai{2}, E. Adams{2}, S. Cohen{2}, Eric Liniger{2}, Chao-Kun Hu{2}, Yann Mignot{4}, A. Grill{2}, Terry Spooner{2}
{1}Global Foundries, United States; {2}IBM, United States; {3}Renesas Electronics Corporation, Japan; {4}STMicroelectronics, United States

<Abstract>
UV cure on robust low-k with sub-nm pore and high carbon content (R-ELK=Robust ELK) was studied to enhance the modulus of the film. UV cure helps to create Si-CH2-Si bridging bond, which plays a role to enhance the modulus. UV cure does not affect the advantage of low PID (plasma-induced damage) and it was confirmed by Cint (interconnect capacitance) measurement for 80 nm pitch interconnect. Besides, UV cured R-ELK demonstrated high TDDB and EM reliability, with lifetime similar to the mature ULK baseline. High TDDB reliability with further dimensional scaling was also confirmed for the test structure with 20 nm spacing.

09:55-10:20

10-3 ***New Fluorocarbon Free Chemistry Proposed As Solution to Limit Porous SiOCH Film Modification During Etching***

Nicolas Posseme{2}, Laurent Vallier{3}, Chia-Ling Kao{1}, Christophe Licitra{2}, Camille Petit-Etienne{3}, Cedric Mannequin{3}, Patrice Gonon{3}, Sergey Belostotskiy{1}, Jerehmia Pender{1}, Sebastien Barnola{2}, Olivier Joubert{3}, Srinivas Nemani{1}
{1}AMAT, United States; {2}CEA-LETI, France; {3}CNRS-LTM, France

<Abstract>
Today porous SiOCH combined with metallic hard masking strategy is an integration of choice for advanced BEOL interconnect technology node. However in this context the main integration issue is the dielectric film sensitivity to fluorocarbon (FC) etch chemistry. In this study, new FC free etching chemistry has been proposed as breakthrough solution. Based on pattern and blanket film analyses, the benefits of this new chemistry is presented and discussed with respect to conventional FC etching. Its compatibility with metallic hard mask integration and wet cleaning is also evaluated.

10:20-10:40 Break

10:40-11:30

Session 11: Process Integration III
Session Co-chairs:
Susumu Matsumoto, Panasonic Corp.
Nae-In Lee, Samsung Electronics Co., Ltd.

10:40-11:05
11-1 ***CVD-Co/Cu(Mn) Integration and Reliability for 10 nm Node***

Takeshi Nogami{2}, Ming He{1}, Xunyuan Zhang{1}, Kunaljeet Tanwar{1}, Raghuveer Patlolla{1}, James Kelly{2}, David Rath{2}, Mahadevaiyer Krishnan{2}, Xuan Lin{1}, Oscar Straten{2}, Hosadurga Shobha{2}, Juntao Li{2}, A. Madan{2}, P. Flaitz{2}, C. Parks{2}, Chao-Kun Hu{2}, C. Penny{2}, A. Simon{2}, T. Bolom{1}, J. Maniscalco{2}, D. Canaperi{2}, Terry Spooner{2}, D. Edelstein{2}
{1}Global Foundries Inc., United States; {2}IBM Corp., United States

<Abstract>
The mechanism of Co liner enhancement of Cu gap-fill was identified to be a wetting improvement of the PVD Cu seed, rather than a local nucleation enhancement for Cu plating. Co gdivot h (top-corner slit void defect) formation can be suppressed by a new wet chemistry, in turn eliminating divot-induced EM degradation. Cu-alloy seed proportional resistivity impact decreased relatively compared to scattering at scaled dimensions. Oxygen at the TaN/CVD-Co interface consumes Mn atoms to diminish Mn segregation at the Cu/cap interface and EM benefits. O-free CVD-Co may solve this problem enabling CVD-Co/Cu-alloy seed integration in advanced nodes.

11:05-11:30
11-2 ***Demonstration of a 12 nm-Half-Pitch Copper Ultralow-K Interconnect Process***

Jasmeet Chawla, Ramanan Chebiam, Rohan Akolkar, Gary Allen, Colin Carver, James Clarke, Florian Gstrein, Michael Harmes, Tejaswi Indukuri, Christopher Jezewski, B. Krist, H. Lang, A. Myers, Richard Schenker, K. J. Singh, R. Turkot, Hui Jae Yoo
Intel, United States

<Abstract>
A process to achieve 12 nm half-pitch interconnect structures in ultralow-k interlayer dielectric (ILD) is realized by pitch division using standard 193 nm lithography. An optimized pattern transfer that minimizes unwanted distortion of ILD features is followed by copper fill. Cross section images and electrical measurements that validate functionality of the drawn structures are presented.

11:30-12:45 Lunch

12:45-15:05

Session 12: 3D Integration II

Session Co-chairs:
Tetsu Tanaka, Tohoku University
Kenichi Takeda, Hitachi

12:45-13:15

12-1 ***INVITED - Development of 3D-stacked Reconfigurable Spin Logic Chip using Via-last Backside-via 3D Integration Technology***

Tetsu Tanaka
Tohoku University, Japan

<Abstract>
The paper will cover process technology of ultrafast on-chip SPRAM and 3D-stacked structure as well as performance of reconfigurable logic chip using the 3D LSI which could overcome the drawbacks of conventional reconfigurable LSIs. The proposed 3D-LSI consists of several reconfigurable spin logic layers with on-chip SPRAMs and processor array layer. These layers are stacked and connected with high density Through-Si Vias (TSVs). This combination could provide both high-speed circuit configuration and parallel reconfiguration. The paper will highlight key process technologies including back-side TSV formation to SPRAM chip and low temperature microbump connection.

13:15-13:40

12-2 ***Novel Through-Silicon via Technologies for 3D System Integration***

Paragkumar Thadesar, Ashish Dembla, Devin Brown, Muhannad Bakir
Georgia Institute of Technology, United States

<Abstract>
To circumvent the performance and energy bottlenecks due to interconnects, novel interconnect solutions are needed both at the package and die levels. This paper reports (1) novel photodefined polymer-embedded vias within silicon interposers for improved through-silicon via insertion loss, and (2) ultrahigh density low-capacitance nanoscale TSVs with 100 nm diameter and 20:1 aspect ratio for fine grain 3D IC implementation.

13:40-14:10

12-3 ***INVITED - Interconnection Requirements and Multi-Die Integration for FPGAs***

Arif Rahman, J. Schulz, R. Grenier, K. Chanda, M.J. Lee, D. Ratakonda, H. Shi, Z. Li, K. Chandrasekar, J. Xie, and D. Ibbotson
Altera, United States

<Abstract>
Die stacking technology with high-density interconnect is enabling new product architectures and capabilities. Silicon interposer based stacking with through silicon via (TSV) has gained traction for high performance applications. Some of the challenges in manufacturing technology, supply-chain strategy, design tools and infrastructure are being addressed to enable broader technology adoption. This paper provides an overview of Field Programmable Gate Array (FPGA) application trends which are driving the need for advanced die-stacking technologies. We present design and manufacturing considerations for stacking technologies and highlight lessons learned from a recent technology demonstration vehicle.

14:10-14:35

12-4 ***System-Level Analysis for 3D Interconnection Networks***

Chenyun Pan, Azad Naeemi
Georgia Institute of Technology, United States

<Abstract>

This paper provides a fast and efficient approach to analyze and compare systems implemented with through-silicon via (TSV) and monolithic inter-tier via (MIV) 3D integration technologies based on compact models for cycle-per-instruction, memory throughput, and multi-level interconnect networks. Additionally, the impact of via diameter and capacitance on the overall system throughput has been quantified. It is demonstrated that for the same die area and thermal constraint, an MIV-based processor offers over 25% improvement in computational throughput as compared with its 2D counterpart.

14:35-15:05

12-5 ***INVITED - 3D Integration challenges today: From technological toolbox to industrial prototypes***

Thierry Mourier
Leti, France

<Abstract>

3D Integration challenges today: From technological toolbox to industrial prototypes 3D integration has been widely described and studied during past years and technological modules and processes were developed for a wide range of applications requested from industry. Today, the integration maturity has reached a manufacturing worthy state and several demonstrators were realized for various products such as advanced interposers, Memory on Logic for mobile applications as well as small volume specific requests for integrated sensors. The talk (or paper) will present the challenges assessed by the toolbox concept in terms of design, modelization and technological modules, discuss on the definition and ramp up of a complete pilot line dedicated to prototyping of 3D demonstrators for various applications from industrial partners and designed to be compatible with processing of wafers coming from and going back to manufacturing facilities. Then, results of fully functional demonstrators obtained through 3D integration and issued from this 300 mm pilot line will be presented and detailed.

15:05-15:20 Break

15:20-17:00

Session 13: Novel Materials & Process II

Session Co-chairs:
Zsolt Tokei, IMEC
Andreas Klipp, BASF Electronic Materials

15:20-15:45

13-1 ***Graphene Interconencts Selectively Grown on Catalytic Metal Damascene Structure and its Growth Mechanism on Ni Catalyst***

Makoto Wada, Taishi Ishikura, Daisuke Nishide, Ban Ito, Yuichi Yamazaki, Tatsuro Saito, Atsunobu Isobayashi, Munehito Kagaya, Takashi Matsumoto, Masayuki Kitamura, Atsuko Sakata, Masahito Watanabe, Naoshi Sakuma, Akihiro Kajita, Tadashi Sakai
Low-power Electronics Association and Project (LEAP), Japan

<Abstract>

The present work investigated the possibility of the formation of graphene interconnects and studied the behavior of graphene growth in wiring structure. Graphene nucleated on the facet of catalytic metal, and multi layer graphene grew

along the terrace surface of catalytic metal. Selective graphene growth served the stacked interconnects structure of graphene / Ni catalytic metal. Reducing surface roughness and controlling graphene growth condition are important to achieve large quantities and high continuity graphene growth.

15:45-16:10

13-2 ***Intercalated Multi-Layer graphene Grown by CVD for LSI Interconnects***

Daiyu Kondo, Haruhisa Nakano, Bo Zhou, Ichiro Kubota, Kenjiro Hayashi, Katsunori Yagi, Makoto Takahashi, Motonobu Sato, Shintaro Sato, Naoki Yokoyama
Collaborative Research Team Green Nanoelectronics Center (GNC),AIST, Japan

<Abstract>
We have fabricated multi-layer graphene (MLG) wiring and demonstrated a resistivity of the same order as Cu and reliability better than Cu. The MLG was synthesized epitaxially by chemical vapor deposition (CVD) on an epitaxial Co film, resulting in quality and electrical properties as good as those of a graphite crystal. The MLG was further intercalated with FeCl3 to achieve a resistivity as low as 9.1 ƒÊƒ¶cm. Our results show that intercalated MLG is really promising for future LSI interconnects.

16:10-16:35

13-3 ***Electrical Improvement of CNT Contacts with Cu Damascene Top Metallization***

Marleen van der Veen{1}, Yohan Barbarin{1}, Bart Vereecke{1}, Masahito Sugiura{2}, Yusaku Kashiwagi{2}, Daire Cott{1}, Cedric Huyghebaert{1}, Zsolt Tökei{1}
{1}imec, Belgium; {2}Tokyo Electron Ltd., Japan

<Abstract>
We discuss the improvement in the electrical characterization and the performance of 150 nm diameter contacts filled with carbon nanotubes (CNT) and a Cu damascene top metal on 200mm wafers. The excellent agreement between the yield curves for the parallel and single contacts shows that a reliable electrical characterization is obtained. We demonstrate that integration changes improved the resistivity of the CNT contact significantly by reducing it from $11.8\cdot10^{3}$ μΩ·cm down to $5.1\cdot10^{3}$ μΩ·cm. Finally, a length scaling of the CNT contacts was used to find the individual contributors to the lowering of the single CNT contact resistance.

16:35-17:00

13-4 ***Carbon Nanotube vias Fabricated at Back-End of Line Compatible Temperature Using a Novel Coal Catalyst***

Sten Vollebregt, Hugo Schellevis, Kees Beenakker, Ryoichi Ishihara
Delft University of Technology, Netherlands

<Abstract>
Vertically aligned carbon nanotubes (CNT) were fabricated using a novel CoAl catalyst at substrate temperatures as low as 350 C and analysed using Raman spectroscopy. Electrical measurement structures were fabricated and characterized using CNT bundles grown at 400 C. The resulting I-V characteristics display a slight non-linearity, likely due to a non-optimal top contact. The first measurement results indicate CoAl can be an attractive candidate for back-end integration of CNT.