IITC 2013 Program At-a-glance

Date	Time	Session	Exhibits
June 13, 2013	8:00	Registration starts	
	09:00-09:10	Opening	
	09:10-10:10	Session 1: Plenary Session	
	10:10-10:25	Break	
	10:25-12:10	Session 2: Process Integration I	
	12:10-13:40	Lunch	**12:10-18:00** **Exhibit Hall Open**
	13:40-15:25	Session 3: Reliability	
	15:25-15:45	Break	
	15:45-18:00	Session 4: Packaging	
June 14, 2013	8:30	Registration starts	**9:00-18:00** **Exhibit Hall Open**
	09:00-10:20	Session 5: Unit Process I	
	10:20-10:40	Break	
	10:40-12:00	Session 6: Unit Process II	
	12:00-13:30	Lunch	
	13:30-15:00	Session 7: Poster session	
	15:00-16:20	Session 8: 3D Integration I	
	16:20-16:40	Break	
	16:40-18:00	Session 9: Novel Materials & Process I	
June 15, 2013	8:30	Registration starts	**9:00-12:00** **Exhibit Hall Open**
	09:00-10:20	Session 10: Process Integration II	
	10:20-10:40	Break	
	10:40-11:30	Session 11: Process Integration III	
	11:30-12:45	Lunch	
	12:45-15:05	Session 12: 3D Integration II	
	15:05-15:20	Break	
	15:20-17:00	Session 13: Novel Materials & Process II	

2013 IEEE International Interconnect Technology Conference
June 13-15, 2013 Kyoto Research Park, Kyoto, Japan

IITC 2013 Program Schedule

Date	Time	Session	Start	End	#	Title	Primaly Author	Affiliation	Region	Exhibits
	09:00-09:10	Opening	09:00	09:10		Welcome and Introduction				
	09:10-10:10	Session 1: Plenary Session	09:10	10:10	1-1	**Keynote Presentation:** Innovative Wafer-based Interconnect Enabling System Integration and Semiconductor Paradigm Shifts	Douglas Chen-Hua Yu	Taiwan Semiconductor Manufacturing Co., Ltd.	Taiwan	
	10:10-10:25	Break	10:10	10:25						
	10:25-12:10	Session 2: Process Integration I	10:25	10:55	2-1	**INVITED -** Spanning the Spectrum of Interconnects: From Trenches of Double Patterning to System Level	Nagaraj N. S.	University of Texas at Dallas	United States	
			10:55	11:20	2-2	Subtractive W Contact and Local Interconnect Co-Integration (CLIC)	Fei Liu	IBM T. J. Watson Research Center	United States	
			11:20	11:45	2-3	CVD Mn-Based Self-Formed Barrier for Advanced Interconnect Technology	Yong Kong Siew	Imec vzw	Belgium	
			11:45	12:10	2-4	Reliable Integration of Robust Porous Ultra Low-k (ULK) for the Advanced BEOL Interconnect	Kyu-Hee Han	Samsung Electronics	Korea	
	12:10-13:40	Lunch	12:10	13:40						
	13:40-15:25	Session 3: Reliability	13:40	14:10	3-1	**INVITED -** The Electromigration Short " Length Effect and Its Impact on Circuit Reliability	A.S. Oates	Taiwan Semiconductor Manufacturing Co., Ltd.	Taiwan	
			14:10	14:35	3-2	Critical Initial Void Growth for Electromigration: Stress Modeling and Multi-Link Statistics for Cu/Low-K Interconnects	Zhuojie Wu	The University of Texas at Austin	United States	
			14:35	15:00	3-3	Void Nucleation and Growth During Electromigration in 30 nm Wide Cu Lines: Impact of Different Interfaces on Failure Mode	Tomoyuki Kirimura	Fujitsu Semiconductor Europe	Belgium	
			15:00	15:25	3-4	AC and Pulsed-DC Stress Electromigration Failure Mechanisms in Cu Interconnects	Ming-Hsien Lin	Taiwan Semiconductor Manufacturing Company. Ltd.	Taiwan	
	15:25-15:45	Break	15:25	15:45						
	15:45-18:00	Session 4: Packaging	15:45	16:15	4-1	**INVITED -** Experimental Analysis of Mechanical Stresses and Material Properties in Multi-Layer Interconnect Systems by fibDAC	Dietmar Vogel	Fraunhofer ENAS, Micro Materials Center;	Germany	12:10-18:00 Exhibit Hall Open
			16:15	16:40	4-2	Modeling of Interconnect Stress Evolution During BEOL Process and Packaging	Xiaopeng Xu	Synopsys, Inc.	United States	
			16:40	17:10	4-3	**INVITED -** CPI Challenges in Advanced Si Technology Nodes	Hang Ping Pu	Taiwan Semiconductor Manufacturing Co., Ltd.	Taiwan	
			17:10	17:35	4-4	A Simple Model-Base Prediction Method for Delamination Failures in Low-K/Cu Interconnects with Flip Chip Packages	Jun Kawahara	Renesas Electronics Corporation	Japan	
			17:35	18:00	4-5	Tier-Independent Microfluidic Cooling for Heterogeneous 3D ICs with Nonuniform Power Dissipation	Yue Zhang	Georgia Institute of Technology	United States	

Date		Session	Start	End	#	Title	Primaly Author	Affiliation	Region	Exhibits
	09:00-10:20	Session 5: Unit Process I	09:00	09:30	5-1	**INVITED -** Damage Free Cryogenic Etching of Ultra Low-k Materials	Mikhail Baklanov	IMEC	Belgium	
			09:30	09:55	5-2	Extremely Non-Porous Ultra-Low-K SiOCH (k=2.3) with Sufficient Modulus (>10 GPa), High Cu Diffusion Barrier and High Tolerance for Integration Process Formed by Large-Radius Neutral-Beam Enhanced CVD	Yoshiyuki Kikuchi	Tokyo Electron Technology and Development Institute	Japan	
			09:55	10:20	5-3	Macroscopic and Microscopic Interface Adhesion Strength of Copper Damascene Interconnects	Nobuyuki Shishido	Nagoya Institute of Technology	Japan	
	10:20-10:40	Break	10:20	10:40						
	10:40-12:00	Session 6: Unit Process II	10:40	11:10	6-1	**INVITED -** Grain Boundary and Surface Scattering in Interconnect Metals	Kevin R. Coffey	University of Central Florida	United States	
			11:10	11:35	6-2	Deposition Behavior and Substrate Dependency of ALD MnOx Diffusion Barrier Layer	Kenji Matsumoto	Tokyo Electron Ltd.	Japan	
			11:35	12:00	6-3	Pore-Sealing Process Initiated by Self-Assembled Layer for Extreme Low-K SiOCH (k=2.0)	Akiko Kobayashi	ASM	Japan	
	12:00-13:30	Lunch	12:00	13:30						
	13:30-15:00	Session 7: Poster session	13:30		7-1	Early Screening Method of Chip-Package Interaction for Multi-Layer Cu/Low-K Structure Using High Load Indentation Test	Tatsuya Usami	Renesas Electronics Corporation	Japan	
					7-2	Early Failure of Short-Lead Metal Line and its Em Characterization with Wheatstone Bridge Test Structure in Advanced Cu/ULK BEOL Process	Tae-Young Jeong	Samsung Electronics Co. LTD	Korea	
					7-3	Redundancy Method to Assess Electromigration Lifetime in Power Grid Design	Boukary Ouattara	STMicroelectronics/Laboratory of Computer Sciences, Paris 6 (LIP6)	France	
					7-4	Compact Modeling and Optimization of Fine-Pitch Interconnects for Silicon Interposers	Vachan Kumar	Georgia Institute of Technology	United States	
					7-5	Low Temperature Bonding of Sn/In-Cu Interconnects for Three-Dimensional Integration Applications	Ruoh-Ning Tzeng	National Chiao Tung University	Taiwan	
					7-6	Thin Nickel Films Growth Using Plasma Enhanced Atomic Layer Deposition from η^3-2-methylallyl N,N'-diisopropylacetamidinate Nickel(II)	Jiro Yokota	Air Liquide Laboratories	Japan	
					7-7	Annealing Effect on the Structure Characteristics of Nano-Scale Damascene Copper Lines	Tatyana Konkova	Ibaraki University	Japan	
					7-8	Endpoint Detection Using Optical Emission Spectroscopy in TSV Fabrication	Ja Myung Gu	Myoungji University	Korea	
June 14, 2013					7-9	WITHDRAW				9:00-18:00 Exhibit Hall Open

IITC 2013 Program Schedule

Date	Time	Session	Start	End	#	Title	Primaly Author	Affiliation	Region	Exhibits
June 15, 2013					7-10	Beam-Substrate Interaction During Tungsten Deposition by Helium Ion Microscope	Kazuyuki Kohama	National Institute of Advanced Industrial Science and Technology (K.Kohama recently moved to JWRI, Osaka University)	Japan	9:00-12:00 Exhibit Hall Open
					7-11	Development and Evaluation of a-SiC:H Films Using a dimethylsilacyclopentane Precursor As a Low-K Cu Capping Layer	Els Van Besien	IMEC	Belgium	
					7-12	Stress Reduction Induced by Bosch Scallops on an Open TSV Technology	Anderson Singulani	Technical University of Vienna	Austria	
					7-13	Fabrication and Electrical Characterization of 5x50um Through Silicon Vias for 3D Integration	Bharat Bhushan	Applied Materials	Singapore	
					7-14	Electrical Properties of Multilayer Graphene Interconnects Prepared by Chemical Vapor Deposition	Masayuki Katagiri	Low-power Electronics Association & Project (LEAP)	Japan	
					7-15	Advanced Nanostructured Materials Applied in Nanoelectronics	Hl Chang	National Chiao Tung University	Taiwan	
					7-16	Numerical Simulations of High Heat Dissipation Technology in LSI 3-D Packaging Using Carbon Nanotube Through Silicon via (CNT-TSV) and Thermal Interface Material (CNT-TIM)	Teppei Kawanabe	Keio University	Japan	
					7-17	Development of Sputtering Technology of Ta_2O_5/TaO_x Stacked Film for ReRAM Mass-Production	Natsuki Fukuda	ULVAC, Inc.	Japan	
	15:00-16:20	Session 8 3D Integration I	15:00	15:30	8-1	**INVITED -** Reliability Challenges of Through-Silicon-Via (TSV) Stacked Memory Chips for 3-D Integration: from Transistors to Packages	Ho-Young Son	SK Hynix	Korea	
			15:30	15:55	8-2	Impact of Material and Microstructure on Thermal Stresses and Reliability of Through-Silicon via (TSV) Structures	Tengfei Jiang	University of Texas at Austin	United States	
			15:55	16:20	8-3	Investigations on Partially Filled HAR TSVs for MEMS Applications	Lutz Hofmann	Fraunhofer Institute for Electronic Nano Systems	Germany	
	16:20-16:40	Break	16:20	16:40						
	16:40-18:00	Session 9: Novel Materials & Process I	16:40	17:10	9-1	**INVITED -** Interconnects with Single Conjugated Polymers	Yuji Okawa	National Institute for Materials Science (NIMS)	Japan	
			17:10	17:35	9-2	A 0.9um Pixel Size Image Sensor Realized by Introducing Organic Photoconductive Film Into the BEOL Process	Shunsuke Isono	Panasonic Corporation	Japan	
			17:35	18:00	9-3	Origin of Large Contact Resistance in Organic Field-Effect Transistors	Takeo Minari	NIMS	Japan	
	09:00-10:20	Session 10: Process Integration II	09:00	09:30	10-1	**INVITED -** 48nm pitch Cu Dual-Damascene Interconnects using Self Aligned Double Patterning Scheme	Shyng-Tsong Chen	IBM Corporation	United States	
			09:30	09:55	10-2	UV Cure Impact on Robust Low-K with Sub-nm Pores and High Carbon Content for High Performance Cu/Low-K BEOL Modules	Naoya Inoue	Renesas Electronics Corporation	United States	
			09:55	10:20	10-3	New Fluorocarbon Free Chemistry Proposed As Solution to Limit Porous SiOCH Film Modification During Etching	Nicolas Posseme	CEA-LETI	France	
	10:20-10:40	Break	10:20	10:40						
	10:40-11:30	Session 11: Process Integration III	10:40	11:05	11-1	CVD-Co/Cu(Mn) Integration and Reliability for 10 nm Node	Takeshi Nogami	IBM Corporation	United States	
			11:05	11:30	11-2	Demonstration of a 12 nm-Half-Pitch Copper Ultralow-K Interconnect Process	Jasmeet Chawla	Intel Corporation	United States	
	11:30-12:45	Lunch	11:30	12:45						
	12:45-15:05	Session 12: 3D Integration II	12:45	13:15	12-1	**INVITED -** Development of 3D-stacked Reconfigurable Spin Logic Chip using Via-last Backside-via 3D Integration Technology	Tetsu Tanaka	Tohoku Univ.	Japan	
			13:15	13:40	12-2	Novel Through-Silicon via Technologies for 3D System Integration	Paragkumar Thadesar	Georgia Institute of Technology	United States	
			13:40	14:10	12-3	**INVITED -** Interconnection Requirements and Multi-Die Integration for FPGAs	Arif Rahman	Altera	United States	
			14:10	14:35	12-4	System-Level Analysis for 3D Interconnection Networks	Chenyun Pan	Georgia Institute of Technology	United States	
			14:35	15:05	12-5	**INVITED -** 3D Integration Challenges Today: From Technological Toolbox to Industrial Prototypes	Thierry Mourier	CEA-LETI	France	
	15:05-15:20	Break	15:05	15:20						
	15:20-17:00	Session 13: Novel Materials & Process II	15:20	15:45	13-1	Graphene Interconencts Selectively Grown on Catalytic Metal Damascene Structure and its Growth Mechanism on Ni Catalyst	Makoto Wada	Low-power Electronics Association and Project	Japan	
			15:45	16:10	13-2	Intercalated Multi-Layer graphene Grown by CVD for LSI Interconnects	Daiyu Kondo	AIST	Japan	
			16:10	16:35	13-3	Electrical Improvement of CNT Contacts with Cu Damascene Top Metallization	Marleen van der Veen	IMEC	Belgium	
			16:35	17:00	13-4	Carbon Nanotube vias Fabricated at Back-End of Line Compatible Temperature Using a Novel CoAl Catalyst	Sten Vollebregt	Delft University of Technology	Netherlands	